phyCORE-Blackfin/BF537

HARDWARE MANUAL

EDITION MAY 2007

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PREFACE

This phyCORE-BF537 Hardware Manual describes the single board computer's design and functions. Precise specifications for the Analog Devices ADSP-BF537 processor can be found in the enclosed processor Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" preceding the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-BF537

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-BF537 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1 INTRODUCTION

The phyCORE-BF537 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-BF537 is a subminiature (84 x 59 mm) insert-ready Single Board Computer populated with the Analog Devices ADSP-BF537 processor. Its universal design enables its insertion in a wide range of embedded applications. All processor signals and ports extend from the processor to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the processor populating the board can be found in the applicable processor User's Manual or datasheet. The descriptions in this manual are based on the Analog Devices Blackfin/ADSP-BF537. No description of compatible processor derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-BF537.

The phyCORE-BF537 offers the following features:

- Insert-ready, subminiature (84 x 59 mm) Single Board Computer subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Analog Devices ADSP-BF537 processor (208-ball MBGA packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to two 200-pin high-density (0.635 mm) Molex connectors aligning two sides of the board, enabling it to be plugged like a "big chip" into target application
- max. 500 MHz clock frequency with up to 1000 MMACs
- Memory Management Unit (MMU), Memory and DMA controllers
- 4 MB external address space, with bus buffers to condition and protect signal load of peripherals on Blackfin external bus interface unit (EBIU)
- 1 (to 4) MB on-board NOR Flash, no dedicated Flash programming voltage required through use of 3.3 V Flash devices
- 16 (to 128) MB SDRAM on-board at 133 MHz
- 32 KByte I2C-EEPROM
- On-chip CAN controller, Philips TJA1041 CAN transceiver on Carrier Board
- 10/100 Mbit/s Ethernet MAC and SMSC LAN8700I Ethernet PHY supporting HP Auto-MDIX
- High Speed USB 2.0 device controller
- PPI supporting ITU-R 656 video data formats
- I²C / 2 x I²S
- SPI
- two UARTS (RS-232 or IrDA), on-board MAX3232 RS-232 transceiver for two channels
- RTC and watchdog timer
- On-board 8-channel, 12-bit AD7927 ADC enabling digitization of analog input values
- Altera FPGA device (max 8256 logic elements)
- JTAG interface for debugging and download of user code
- Single supply 3.3V with on-board power management
- Industrial temperature range (-40°...+85°C)[1]

[1]: Only valid for units without USB controller. Temperature range reduced to 0 - 70°C with USB controller installed.

1.1 Block Diagram

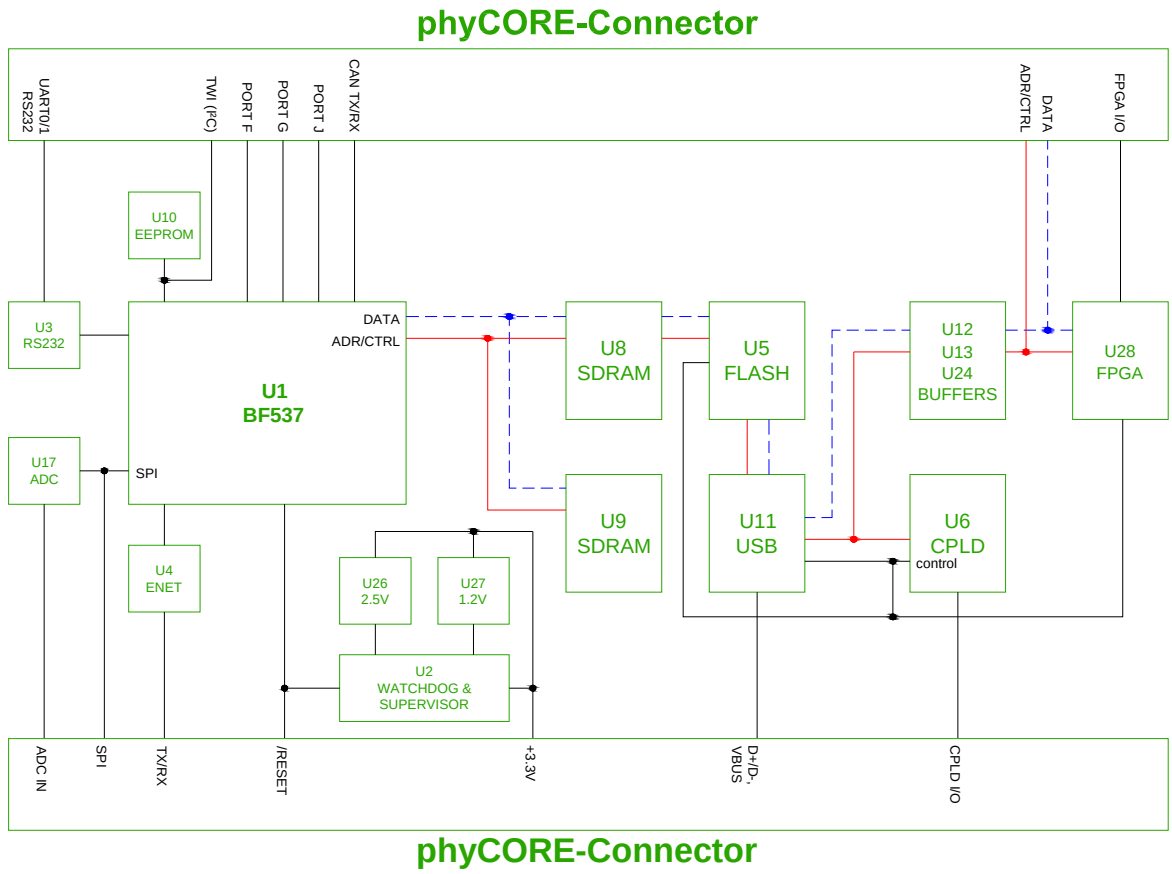

Figure 1: Block Diagram phyCORE-BF537

1.2 VIEW OF THE phyCORE-BF537

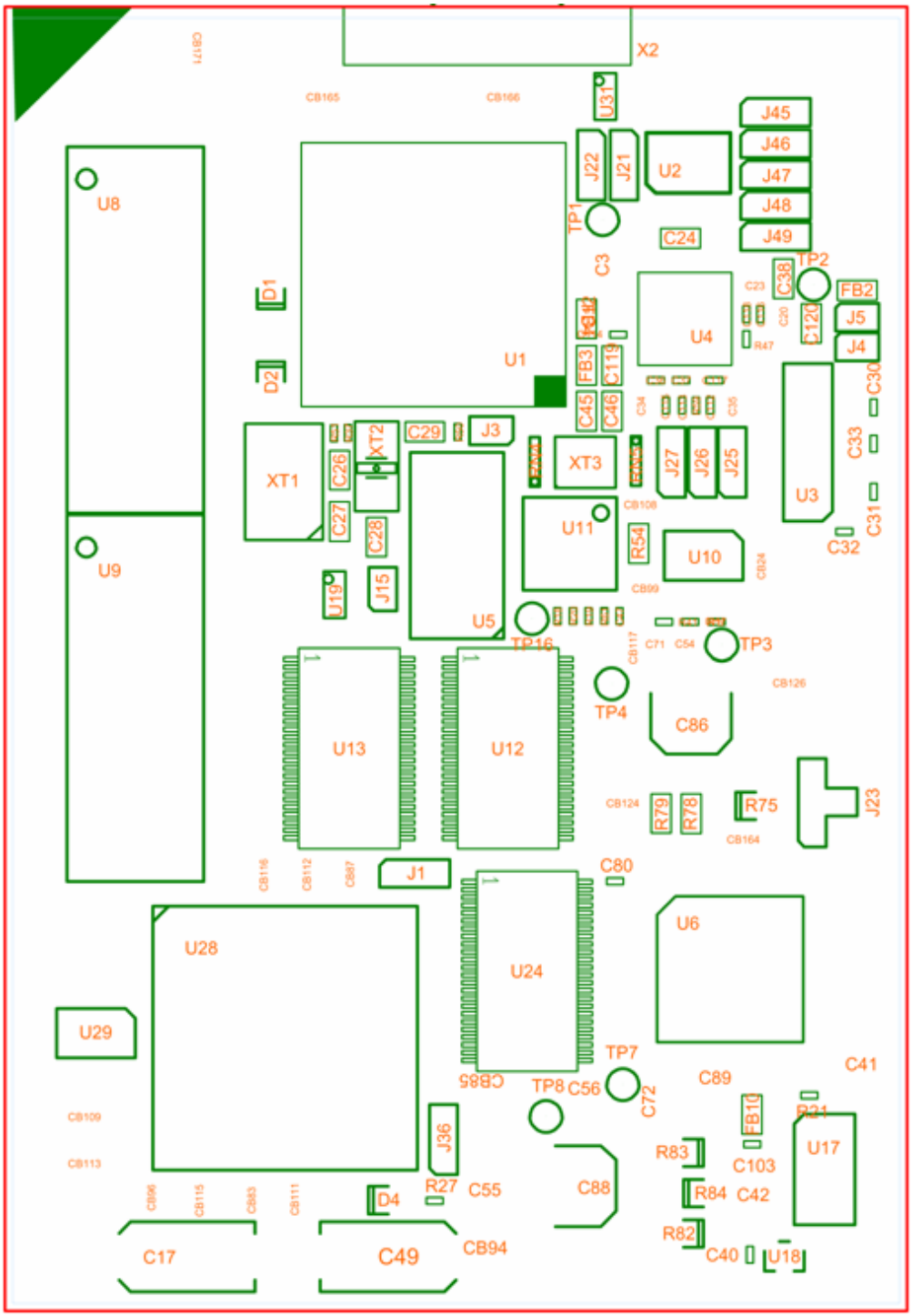

Figure 2: Top View of the phyCORE-BF537 (controller side)

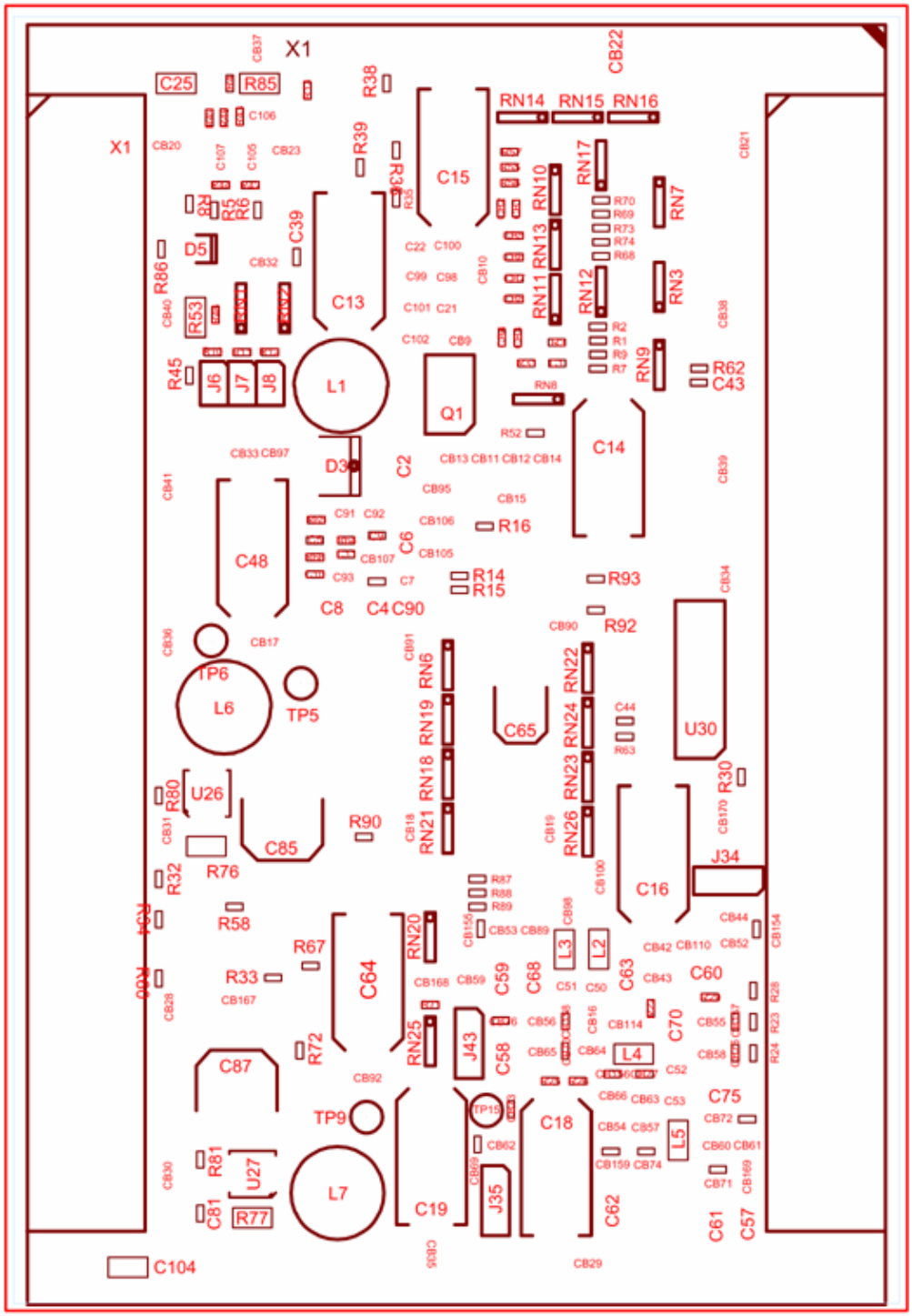

Figure 3: Bottom View of the phyCORE-BF537 (connector side)

2 PIN DESCRIPTION

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-BF537 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Carrier Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-BF537 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-BF537 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module’s phyCORE-connector as well as mating connectors on the phyCORE Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector. The location of row 1 on the board is marked by a white triangle on the PCB to allow easy identification.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-BF537 with SMT phyCORE-connectors on its underside (defined as dotted lines) mounted on a Carrier Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCORE module showing these phyCORE-connectors mounted on the underside of the module’s PCB.

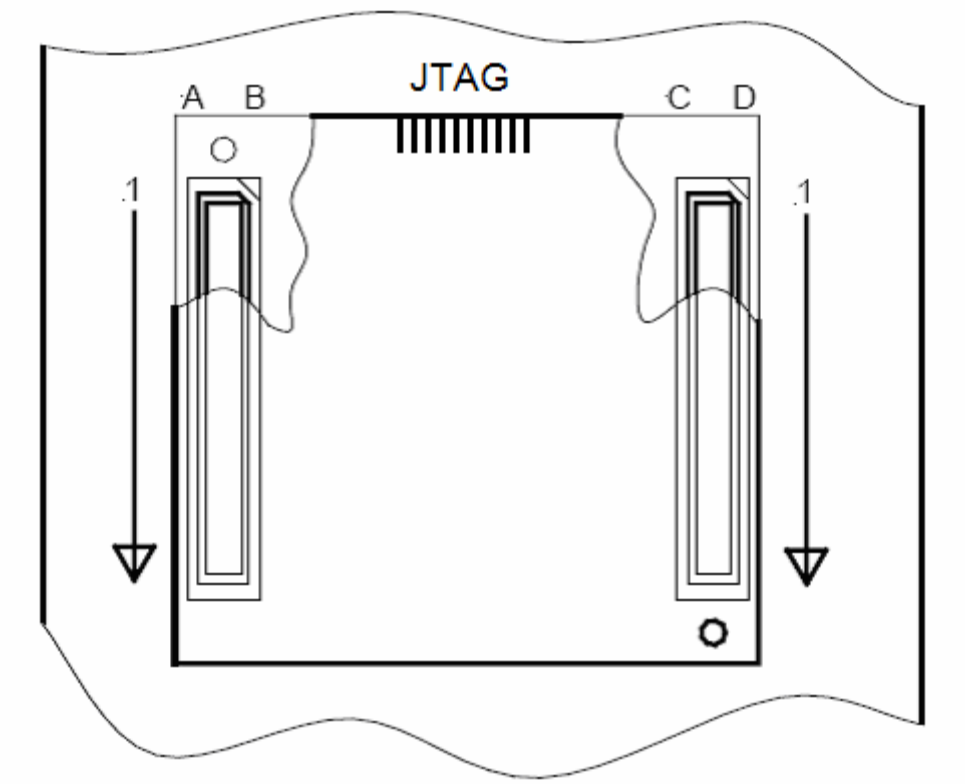

Figure 4: Pinout of the phyCORE-Connector (Top View, with Cross Section Insert)

Table 1 provides an overview of the pinout of the phyCORE-connector, as well as descriptions of possible alternative functions. The signal direction in the I/O column is consistent with the default phyCORE-BF537 population options. For instance, although PF6 is a bidirectional processor port signal, on the phyCORE-BF537 this signal is used to generate the /USB_RESET signal connected to the USB device controller. In this case PF6 is a designated as an output in the I/O column, despite PF6 of the processor being bidirectional. Keep in mind that if the USB section was not populated then this signal could be used as a bidirectional I/O.

Please refer to the Analog Devices ADSP-BF537 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Table 1: Pinout of the phyCORE-Connector X1

PIN ROW X1A			
PIN #	SIGNAL	I/O	DESCRIPTION
1A	N/C	-	Not Connected
2A	GND	-	Ground
3A	N/C	-	Not connected
4A	/NMI	-	Processor signal /NMI
5A	/BUF_AMS0	-	Buffered processor signal /AMS0
6A	/BUF_AMS2	-	Buffered processor signal /AMS2
7A	GND	-	Ground
8A	/BUF_AWE	O	Buffered processor signal /AWE
9A	BUF_A1	O	Buffered processor signal A1
10A	BUF_A2	O	Buffered processor signal A2
11A	BUF_A4	O	Buffered processor signal A4
12A	GND	-	Ground
13A	BUF_A7	O	Buffered processor signal A7
14A	BUF_A9	O	Buffered processor signal A9
15A	BUF_A10	O	Buffered processor signal A10
16A	BUF_A12	O	Buffered processor signal A12
17A	GND	-	Ground
18A	BUF_A15	O	Buffered processor signal A15
19A	BUF_D1	I/O	Buffered processor signal D1
20A	BUF_D2	I/O	Buffered processor signal D2
21A	BUF_D4	I/O	Buffered processor signal D4
22A	GND	-	Ground
23A	BUF_D7	I/O	Buffered processor signal D7
24A	BUF_A17	O	Buffered processor signal A17
25A	BUF_A18	O	Buffered processor signal A18
26A	PLD_IO18	I/O	CPLD I/O #18
27A	GND	-	Ground
28A	PLD_IO22	I/O	CPLD I/O #22
29A	BUF_D9	I/O	Buffered processor signal D9
30A	BUF_D10	I/O	Buffered processor signal D10
31A	BUF_D12	I/O	Buffered processor signal D12
32A	GND	-	Ground
33A	BUF_D15	I/O	Buffered processor signal D15
34A	BUF_ARDY	I	Buffered processor signal ARDY
35A	/FPGA_RST1	I	Optional FPGA reset input source
36A	PG0	I/O	Processor PG0: GPIO / PPI data 0
37A	GND	-	Ground

38A	PG2	I/O	Processor PG2: GPIO / PPI data 2
39A	PG4	I/O	Processor PG4: GPIO / PPI data 4
40A	PG5	I/O	Processor PG5: GPIO / PPI data 5
41A	PG7	I/O	Processor PG7: GPIO / PPI data 7
42A	GND	-	Ground
43A	PG10	I/O	Processor PG10: GPIO / PPI data 10 / SPORT1 receive serial clock
44A	EXT_PG12	I/O	De-multiplexed processor PG12: GPIO / PPI data 12 / SPORT1 receive data primary
45A	EXT_PG13	I/O	De-multiplexed processor PG13: GPIO / PPI data 13 / SPORT1 transmit serial clock
46A	EXT_PG15	I/O	De-multiplexed processor PG15: GPIO / PPI data 15 / SPORT1 transmit data primary
47A	GND	-	Ground
48A	FPGA_B1_D5	I/O	FPGA bank 1 pin D5
49A	FPGA_B1_E5	I/O	FPGA bank 1 pin E5
50A	FPGA_B1_D4	I/O	FPGA bank 1 pin D4
51A	FPGA_B1_E3	I/O	FPGA bank 1 pin E3
52A	GND	-	Ground
53A	FPGA_B1_F3	I/O	FPGA bank 1 pin F3
54A	FPGA_B1_D1	I/O	FPGA bank 1 pin D1
55A	FPGA_B1_H6	I/O	FPGA bank 1 pin H6
56A	FPGA_B1_G4	I/O	FPGA bank 1 pin G4
57A	GND	-	Ground
58A	FPGA_B1_J2	I/O	FPGA bank 1 pin J2
59A	FPGA_B1_K2	I/O	FPGA bank 1 pin K2
60A	FPGA_B1_K4	I/O	FPGA bank 1 pin K4
61A	FPGA_B1_L1	I/O	FPGA bank 1 pin L1
62A	GND	-	Ground
63A	FPGA_B1_L2	I/O	FPGA bank 1 pin L2
64A	FPGA_B1_M2	I/O	FPGA bank 1 pin M2
65A	FPGA_B1_L3	I/O	FPGA bank 1 pin L3
66A	FPGA_B1_P1	I/O	FPGA bank 1 pin P1
67A	GND	-	Ground
68A	FPGA_B1_P2	I/O	FPGA bank 1 pin P2
69A	FPGA_B1_M4	I/O	FPGA bank 1 pin M4
70A	FPGA_B1_N3	I/O	FPGA bank 1 pin N3
71A	FPGA_B4_N9	I/O	FPGA bank 4 pin N9
72A	GND	-	Ground
73A	FPGA_B4_N10	I/O	FPGA bank 4 pin N10
74A	FPGA_B4_R11	I/O	FPGA bank 4 pin R11
75A	FPGA_B4_R10	I/O	FPGA bank 4 pin R10
76A	FPGA_B4_K11	I/O	FPGA bank 4 pin K11

77A	GND	-	Ground
78A	FPGA_B4_K10	I/O	FPGA bank 4 pin K10
79A	FPGA_B4_P13	I/O	FPGA bank 4 pin P13
80A	FPGA_B4_T13	I/O	FPGA bank 4 pin T13
81A	FPGA_B4_T14	I/O	FPGA bank 4 pin T14
82A	GND	-	Ground
83A	FPGA_B4_R14	I/O	FPGA bank 4 pin R14
84A	FPGA_B4_L11	I/O	FPGA bank 4 pin L11
85A	FPGA_B4_T3	I/O	FPGA bank 4 pin T3
86A	FPGA_B4_P5	I/O	FPGA bank 4 pin P5
87A	GND	-	Ground
88A	FPGA_B4_P4	I/O	FPGA bank 4 pin P4
89A	FPGA_B4_R4	I/O	FPGA bank 4 pin R4
90A	FPGA_B4_T7	I/O	FPGA bank 4 pin T7
91A	FPGA_B4_L7	I/O	FPGA bank 4 pin L7
92A	GND	-	Ground
93A	FPGA_B4_L8	I/O	FPGA bank 4 pin L8
94A	FPGA_B4_R8	I/O	FPGA bank 4 pin R8
95A	FPGA_B4_N8	I/O	FPGA bank 4 pin N8
96A	FPGA_B4_N6	I/O	FPGA bank 4 pin N6
97A	GND	-	Ground
98A	FPGA_B4_K7	I/O	FPGA bank 4 pin K7
99A	FPGA_B4_N6	I/O	FPGA bank 4 pin N6
100A	FPGA_B4_N7	I/O	FPGA bank 4 pin N7

PIN ROW X1B			
PIN #	SIGNAL	I/O	DESCRIPTION
1B	CKLOUT	O	Buffered 25 MHz system crystal
2B	N/C	-	Not connected
3B	N/C	-	Not Connected
4B	GND	-	Ground
5B	/BUF_AMS1	O	Buffered processor signal /AMS1
6B	/BUF_AMS3	O	Buffered processor signal /AMS3
7B	/BUF_ARE	O	Buffered processor signal /ARE
8B	/BUF_AOE	O	Buffered processor signal /AOE
9B	GND	-	Ground
10B	BUF_A3	O	Buffered processor signal A3
11B	BUF_A5	O	Buffered processor signal A5
12B	BUF_A6	O	Buffered processor signal A6
13B	BUF_A8	O	Buffered processor signal A8
14B	GND	-	Ground
15B	BUF_A11	O	Buffered processor signal A11
16B	BUF_A13	O	Buffered processor signal A13
17B	BUF_A14	O	Buffered processor signal A14
18B	BUF_D0	I/O	Buffered processor signal D0
19B	GND	-	Ground
20B	BUF_D3	I/O	Buffered processor signal D3
21B	BUF_D5	I/O	Buffered processor signal D5
22B	BUF_D6	I/O	Buffered processor signal D6
23B	BUF_A16	O	Buffered processor signal A16
24B	GND	-	Ground
25B	BUF_A19	O	Buffered processor signal A19
26B	PLD_IO19	I/O	CPLD I/O #19
27B	PLD_IO21	I/O	CPLD I/O #21
28B	BUF_D8	I/O	Buffered processor signal D8
29B	GND	-	Ground
30B	BUF_D11	I/O	Buffered processor signal D11
31B	BUF_D13	I/O	Buffered processor signal D13
32B	BUF_D14	I/O	Buffered processor signal D14
33B	/BUF_ABE0	O	Buffered processor signal /ABE0
34B	GND	-	Ground
35B	/BUF_ABE1	O	Buffered processor signal /ABE1
36B	/FPGA_RST0	I	Optional FPGA reset input source
37B	PG1	I/O	Processor PG1: GPIO / PPI data 1
38B	PG3	I/O	Processor PG3: GPIO / PPI data 3
39B	GND	-	Ground

40B	PG6	I/O	Processor PG6: GPIO / PPI data 6
41B	PG8	I/O	Processor PG8: GPIO / PPI data 8 / SPORT1 receive data secondary
42B	PG9	I/O	Processor PG9: GPIO / PPI data 9 / SPORT1 transmit data secondary
43B	PG11	I/O	Processor PG11: GPIO / PPI data 11 / SPORT1 receive frame sync
44B	GND	-	Ground
45B	EXT_PG14	I/O	De-multiplexed processor PG14: GPIO / PPI data 14 / SPORT1 transmit frame sync
46B	FPGA_B1_C1	I/O	FPGA bank 1 pin C1
47B	FPGA_B1_C2	I/O	FPGA bank 1 pin C2
48B	FPGA_B1_D3	I/O	FPGA bank 1 pin D3
49B	GND	-	Ground
50B	FPGA_B1_E4	I/O	FPGA bank 1 pin E4
51B	FPGA_B1_E2	I/O	FPGA bank 1 pin E2
52B	FPGA_B1_E1	I/O	FPGA bank 1 pin E1
53B	FPGA_B1_D2	I/O	FPGA bank 1 pin D2
54B	GND	-	Ground
55B	FPGA_B1_J6	I/O	FPGA bank 1 pin J6
56B	FPGA_B1_F5	I/O	FPGA bank 1 pin F5
57B	FPGA_B1_H1	I/O	FPGA bank 1 pin H1
58B	FPGA_B1_J1	I/O	FPGA bank 1 pin J1
59B	GND	-	Ground
60B	FPGA_B1_K1	I/O	FPGA bank 1 pin K1
61B	FPGA_B1_K5	I/O	FPGA bank 1 pin K5
62B	FPGA_B1_M1	I/O	FPGA bank 1 pin M1
63B	FPGA_B1_M3	I/O	FPGA bank 1 pin M3
64B	GND	-	Ground
65B	FPGA_B1_N1	I/O	FPGA bank 1 pin N1
66B	FPGA_B1_N2	I/O	FPGA bank 1 pin N2
67B	FPGA_B1_L4	I/O	FPGA bank 1 pin L4
68B	FPGA_B1_J4	I/O	FPGA bank 1 pin J4
69B	GND	-	Ground
70B	FPGA_B1_P3	I/O	FPGA bank 1 pin P3
71B	FPGA_B1_N4	I/O	FPGA bank 1 pin N4
72B	FPGA_B4_T11	I/O	FPGA bank 4 pin T11
73B	FPGA_B4_L9	I/O	FPGA bank 4 pin L9
74B	GND	-	Ground
75B	FPGA_B4_L10	I/O	FPGA bank 4 pin L10
76B	FPGA_B4_T10	I/O	FPGA bank 4 pin T10
77B	FPGA_B4_P12	I/O	FPGA bank 4 pin P12
78B	FPGA_B4_T12	I/O	FPGA bank 4 pin T12

79B	GND	-	Ground
80B	FPGA_B4_R12	I/O	FPGA bank 4 pin R12
81B	FPGA_B4_R13	I/O	FPGA bank 4 pin R13
82B	FPGA_B4_M11	I/O	FPGA bank 4 pin M11
83B	FPGA_B4_N11	I/O	FPGA bank 4 pin N11
84B	GND	-	Ground
85B	FPGA_B4_P11	I/O	FPGA bank 4 pin P11
86B	FPGA_B4_R3	I/O	FPGA bank 4 pin R3
87B	FPGA_B4_T4	I/O	FPGA bank 4 pin T4
88B	FPGA_B4_T5	I/O	FPGA bank 4 pin T5
89B	GND	-	Ground
90B	FPGA_B4_R5	I/O	FPGA bank 4 pin R5
91B	FPGA_B4_R7	I/O	FPGA bank 4 pin R7
92B	FPGA_B4_T8	I/O	FPGA bank 4 pin T8
93B	FPGA_B4_T9	I/O	FPGA bank 4 pin T9
94B	GND	-	Ground
95B	FPGA_B4_R9	I/O	FPGA bank 4 pin R9
96B	FPGA_B4_T6	I/O	FPGA bank 4 pin T6
97B	FPGA_B4_K6	I/O	FPGA bank 4 pin K6
98B	FPGA_B4_P6	I/O	FPGA bank 4 pin P6
99B	GND	-	Ground
100B	N/C	-	Not connected

PIN ROW X1C			
PIN #	SIGNAL	I/O	DESCRIPTION
1C	VCC_3V3	I	3.3V primary power input supply
2C	VCC_3V3	I	3.3V primary power input supply
3C	GND	-	Ground
4C	ADC_AVCC	I	ADC power supply input
5C	ADC_AVCC	I	ADC power supply input
6C	VBAT	I	Battery supply input
7C	GND	-	Ground
8C	N/C	-	Not connected
9C	N/C	-	Not connected
10C	/RESET	O	Reset output from voltage supervisor
11C	/RESOUT	O	Buffered reset output from voltage supervisor
12C	GND	-	Ground
13C	/USB_RESET	O	Processor PF6: GPIO / Timer 3 / SPI Slave Select Enable 6 – **connected to on-board USB controller; used as USB reset signal**
14C	PF8	I/O	Processor PF8: GPIO / Timer 1 / PPI Frame Sync 2
15C	PF9	I/O	Processor PF9: GPIO / Timer 0 / PPI Frame Sync 1
16C	SPI_MOSI	O	Processor PF11: GPIO / SPI Master Out Slave In – **connected to on-board ADC; used with ADC SPI interface**
17C	GND	-	Ground
18C	SPI_MISO	I	Processor PF12: GPIO / SPI Master In Slave Out – **connected to on-board ADC; used with ADC SPI interface**
19C	UART1_RX	I	Processor PF3: GPIO / UART1 Receive / DMA Request 0 – **connected to on-board RS-232 transceiver; used as UART1 with RS-232 transceiver**
20C	UART1_TX	O	Processor PF2: GPIO / UART1 Transmit / Timer 7 – **connected to on-board RS-232 transceiver; used as UART1 with RS-232 transceiver**
21C	UART1_RX_RS232	I	UART1 receive at RS-232 levels
22C	GND	-	Ground
23C	UART1_TX_RS232	O	UART1 transmit at RS-232 levels
24C	PF14	I/O	Processor PF14: GPIO / SPI Slave Select / Alternate Timer0 Clock Input
25C	AMS3_CTRL	I	Optional asynchronous memory bank 3 select control signal input; only used if default processor signal PF4 is needed for something other than default asynchronous bank 3 control
26C	USB_VBUS	I	USB device controller VBUS input
27C	GND	-	Ground
28C	PLD_IO23	I/O	PLD I/O #23
29C	PLD_IO24	I/O	PLD I/O #24

30C	/FPGA_STATUS	O	FPGA configuration status output
31C	I2C_SCL	I/O	Processor PJ2: I²C Serial Clock – **connected to on-board EEPROM**
32C	GND	-	Ground
33C	LINK	O	Ethernet LINK signal (for LINK LED)
34C	ACTIVITY	O	Ethernet ACTIVITY signal (for ACTIVITY LED)
35C	RXN	I/O	Ethernet differential receive signal RXN
36C	TXN	I/O	Ethernet differential transmit signal TXN
37C	GND	-	Ground
38C	PJ7	I/O	Processor PJ7
39C	PJ9	I/O	Processor PJ9
40C	PJ10	I/O	Processor PJ10
41C	/WD_OFF	I	Watchdog off input signal to the voltage supervisor – connect to GND to disable on-board watchdog
42C	GND	-	Ground
43C	FPGA_B3_G15	I/O	FPGA bank 3 pin G15
44C	FPGA_B3_G16	I/O	FPGA bank 3 pin G16
45C	FPGA_B3_F15	I/O	FPGA bank 3 pin F15
46C	FPGA_B3_J11	I/O	FPGA bank 3 pin J11
47C	GND	-	Ground
48C	FPGA_B3_D16	I/O	FPGA bank 3 pin D16
49C	FPGA_B3_D15	I/O	FPGA bank 3 pin D15
50C	FPGA_B3_C14	I/O	FPGA bank 3 pin C14
51C	FPGA_B3_D14	I/O	FPGA bank 3 pin D14
52C	GND	-	Ground
53C	FPGA_B3_E15	I/O	FPGA bank 3 pin E15
54C	FPGA_B3_C15	I/O	FPGA bank 3 pin C15
55C	FPGA_B3_E13	I/O	FPGA bank 3 pin E13
56C	FPGA_B3_F14	I/O	FPGA bank 3 pin F14
57C	GND	-	Ground
58C	FPGA_B3_J16	I/O	FPGA bank 3 pin J16
59C	FPGA_B3_M12	I/O	FPGA bank 3 pin M12
60C	FPGA_B3_P16	I/O	FPGA bank 3 pin P16
61C	FPGA_B3_N16	I/O	FPGA bank 3 pin N16
62C	GND	-	Ground
63C	FPGA_B3_M15	I/O	FPGA bank 3 pin M15
64C	FPGA_B3_L16	I/O	FPGA bank 3 pin L16
65C	FPGA_B3_K15	I/O	FPGA bank 3 pin K15
66C	FPGA_B3_M14	I/O	FPGA bank 3 pin M14
67C	GND	-	Ground
68C	FPGA_B3_L12	I/O	FPGA bank 3 pin L12
69C	FPGA_B3_K13	I/O	FPGA bank 3 pin K13

70C	FPGA_B3_L14	I/O	FPGA bank 3 pin L14
71C	FPGA_B3_P14	I/O	FPGA bank 3 pin P14
72C	GND	-	Ground
73C	FPGA_TMS	I	FPGA JTAG port signal TMS (test mode select)
74C	FPGA_TDI	I	FPGA JTAG port signal TDI (test data input)
75C	FPGA_TDO	O	FPGA JTAG port signal TDO (test data output)
76C	FPGA_TCK	I	FPGA JTAG port signal TCK (test clock)
77C	GND	-	Ground
78C	PLD_IO4/TDI	I	CPLD I/O #4 / CPLD JTAG port signal TDI (test data input)
79C	PLD_IO9/TMS	I	CPLD I/O #9 / CPLD JTAG port signal TMS (test mode select)
80C	PLD_IO20/TDO	O	CPLD I/O #20 / CPLD JTAG port signal TDO (test data output)
81C	PLD_IO25/TCK	I	CPLD I/O #25 / CPLD JTAG port signal TCK (test clock)
82C	AGND	-	Analog ground
83C	N/C	-	Not connected
84C	N/C	-	Not connected
85C	N/C	-	Not connected
86C	N/C	-	Not connected
87C	AGND	-	Analog ground
88C	N/C	-	Not connected
89C	N/C	-	Not connected
90C	N/C	-	Not connected
91C	N/C	-	Not connected
92C	AGND	-	Analog ground
93C	N/C	-	Not connected
94C	N/C	-	Not connected
95C	N/C	-	Not connected
96C	ADC_IN0	I	Analog-to-digital converter input 0
97C	AGND	-	Analog ground
98C	ADC_IN3	I	Analog-to-digital converter input 3
99C	ADC_IN5	I	Analog-to-digital converter input 5
100C	ADC_IN6	I	Analog-to-digital converter input 6

PIN ROW X1D			
PIN #	SIGNAL	I/O	DESCRIPTION
1D	VCC_3V3	I	3.3V primary power input supply
2D	VCC_3V3	I	3.3V primary power input supply
3D	GND	-	Ground
4D	FPGA_VCCIO	I	FPGA bank I/O voltage select input
5D	FPGA_VCCIO	I	FPGA bank I/O voltage select input
6D	VPD	O	RTC power pin voltage output
7D	PWRGOOD	O	Voltage supervisor power good output
8D	WDI	I	Watchdog input
9D	GND	-	Ground
10D	/RESIN	I	Reset input
11D	PF4	I/O	Processor PF4: GPIO / Timer5 / SPI slave select enable 6
12D	SPI_SSEL5	O	Processor PF5: GPIO / Timer4 / SPI slave select enable 5 – **connected to on-board ADC; used with ADC SPI interface**
13D	/USB_IRQ	O	Processor PF6: GPIO / Timer3 / SPI slave select enable 4 – **connected to on-board USB controller; used as USB interrupt signal**
14D	GND	-	Ground
15D	PF10	I/O	Processor PF10: GPIO / SPI slave select enable 1
16D	UART0_RX	I	Processor PF1: GPIO / UART0 receive / DMA request 1 / Timer1 alternate input capture – **connected to on-board RS-232 transceiver; used as UART0 with RS-232 transceiver**
17D	UART0_TX	O	Processor PF0: GPIO / UART0 transmit / DMA request 0 – **used as UART0 with RS-232- transceiver**
18D	SPI_SCK	O	Processor PF13: GPIO / SPI clock – **connected to on-board ADC; used with ADC SPI interface**
19D	GND	-	Ground
20D	CAN_RX	I	Processor PJ4: SPORT0 receive data secondary / CAN receive / Timer0 alternate input capture
21D	CAN_TX	O	Processor PJ5: SPORT0 transmit data secondary / CAN transmit / SPI slave select enable 7
22D	UART0_RX_RS232	I	UART0 receive at RS-232 levels
23D	UART0_TX_RS232	O	UART0 transmit at RS-232 levels
24D	GND	-	Ground
25D	PF15	I/O	Processor PF15: GPIO / PPI clock / external timer reference
26D	GND	-	Ground
27D	USB_DM	I/O	USB differential signal D minus
28D	USB_DP	I/O	USB differential signal D plus
29D	GND	-	Ground
30D	FPGA_PCTRL	I	FPGA programming control input
31D	I2C_WP	I	I²C write protect input to on-board EEPROM

32D	I2C_SDA	I/O	Processor PJ3: I²C serial data – **connected to on-board EEPROM**
33D	PLD_IO26	I/O	PLD I/O #26
34D	GND	-	Ground
35D	RXP	I/O	Ethernet differential receive signal RXP
36D	TXP	I/O	Ethernet differential transmit signal TXP
37D	PJ6	I/O	Processor PJ6: SPORT0 receive serial clock / alternate Timer2 clock input
38D	PJ8	I	Processor PJ8: SPORT0 receive data primary / alternate Timer4 clock input
39D	GND	-	Ground
40D	PJ11	O	Processor PJ11: SPORT0 transmit data primary / SPI slave select enable 2
41D	BMODE0	I	Boot mode select bit 0
42D	BMODE1	I	Boot mode select bit 1
43D	BMODE2	I	Boot mode select bit 2
44D	GND	-	Ground
45D	/EMU	O	Processor JTAG interface signal /EMU
46D	/TRST	I	Processor JTAG interface signal /TRST
47D	TMS	I	Processor JTAG interface signal TMS
48D	TDI	I	Processor JTAG interface signal TDI
49D	GND	-	Ground
50D	TCK	I	Processor JTAG interface signal TCK
51D	TDO	O	Processor JTAG interface signal TDO
52D	FPGA_B3_J12	I/O	FPGA bank 3 pin J12
53D	FPGA_B3_H12	I/O	FPGA bank 3 pin H12
54D	GND	-	Ground
55D	FPGA_B3_F16	I/O	FPGA bank 3 pin F16
56D	FPGA_B3_H11	I/O	FPGA bank 3 pin H11
57D	FPGA_B3_G13	I/O	FPGA bank 3 pin G13
58D	FPGA_B3_G12	I/O	FPGA bank 3 pin G12
59D	GND	-	Ground
60D	FPGA_B3_D13	I/O	FPGA bank 3 pin D13
61D	FPGA_B3_E14	I/O	FPGA bank 3 pin E14
62D	FPGA_B3_H13	I/O	FPGA bank 3 pin H13
63D	FPGA_B3_E16	I/O	FPGA bank 3 pin E16
64D	GND	-	Ground
65D	FPGA_B3_C16	I/O	FPGA bank 3 pin C16
66D	FPGA_B3_F13	I/O	FPGA bank 3 pin F13
67D	FPGA_B3_H15	I/O	FPGA bank 3 pin H15
68D	FPGA_B3_J15	I/O	FPGA bank 3 pin J15
69D	GND	-	Ground
70D	FPGA_B3_N12	I/O	FPGA bank 3 pin N12

71D	FPGA_B3_P15	I/O	FPGA bank 3 pin P15
72D	FPGA_B3_N15	I/O	FPGA bank 3 pin N15
73D	FPGA_B3_M16	I/O	FPGA bank 3 pin M16
74D	GND	-	Ground
75D	FPGA_B3_L15	I/O	FPGA bank 3 pin L15
76D	FPGA_B3_K16	I/O	FPGA bank 3 pin K16
77D	FPGA_B2_B8	I/O	FPGA bank 2 pin B8
78D	FPGA_B2_D7	I/O	FPGA bank 2 pin D7
79D	GND	-	Ground
80D	FPGA_B2_D9	I/O	FPGA bank 2 pin D9
81D	PLD_IO27	I/O	PLD I/O #27
82D	PLD_IO28	I/O	PLD I/O #28
83D	PLD_IO29	I/O	PLD I/O #29
84D	AGND	-	Analog ground
85D	N/C	-	Not connected
86D	N/C	-	Not connected
87D	N/C	-	Not connected
88D	N/C	-	Not connected
89D	AGND	-	Analog ground
90D	N/C	-	Not connected
91D	N/C	-	Not connected
92D	N/C	-	Not connected
93D	N/C	-	Not connected
94D	AGND	-	Analog ground
95D	N/C	-	Not connected
96D	ADC_IN1	I	Analog-to-digital converter input 1
97D	ADC_IN2	I	Analog-to-digital converter input 2
98D	ADC_IN4	I	Analog-to-digital converter input 4
99D	AGND	-	Analog ground
100D	ADC_IN7	I	Analog-to-digital converter input 7

3 JUMPERS

For configuration purposes, the phyCORE-BF537 has 23 solder jumpers, some of which have been installed prior to delivery. *Figure 5* and *Figure 6* indicate the location of the solder jumpers on the board. All but six solder jumpers are located on the top side of the module (opposite side of connectors).

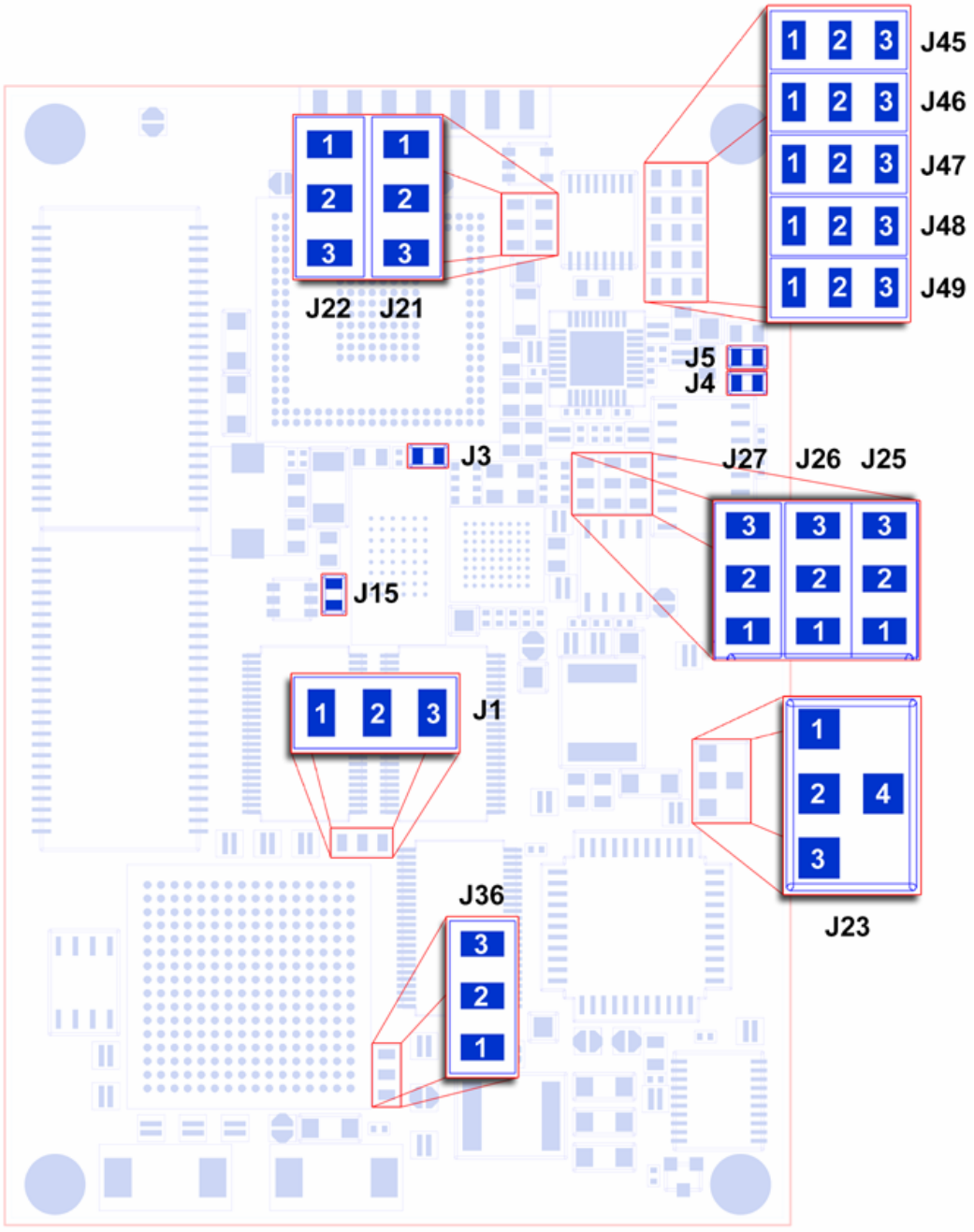

Figure 5: Jumpers Locations (Top View)

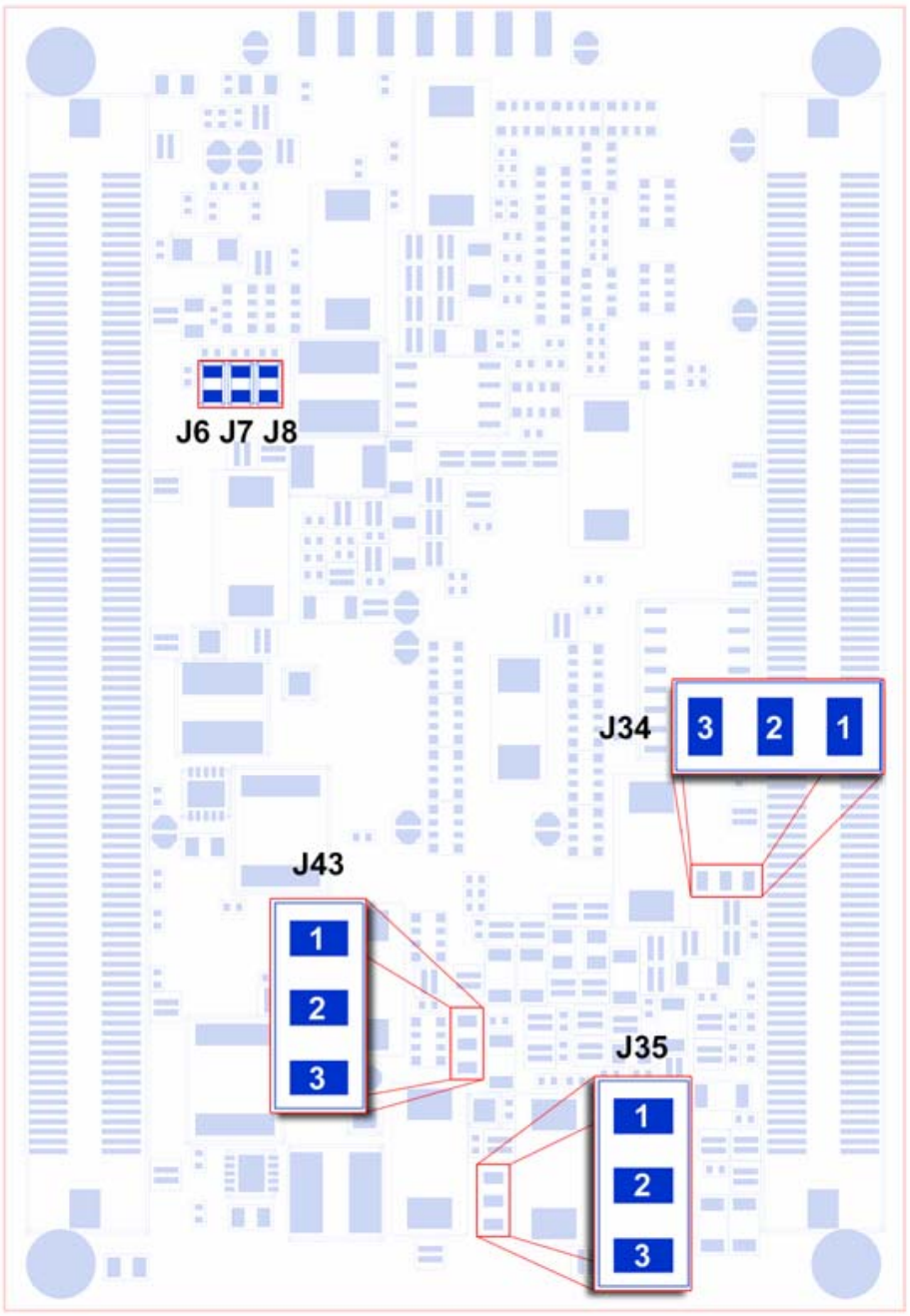

Figure 6: Jumpers Locations (Bottom View)

Table 2 below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper Settings

	Default Setting		Alternative Setting		See Section
J1	2 + 3	Bus buffer direction controlled by the /AOE from the BF537	1 + 2	Bus buffer direction controlled by the BUF_DIR from the CPLD U6	*10*
J3	open	CLKOUT disconnected from CLKBUF	closed	CLKOUT connected to CLKBUF	*3.1*
J4	closed	UART0_RX converted to RS-232 level	open	UART0_RX left at TTL level	*7.1.1*
J5	closed	UART1_RX converted to RS-232 level	open	UART1_RX left at TTL level	
J6	open[1]	Ethernet mode selection bit 0	closed	Ethernet mode selection bit 0 pulled low	*7.2.1*
J7	open[1]	Ethernet mode selection bit 1	closed	Ethernet mode selection bit 1 pulled low	
J8	open[1]	Ethernet mode selection bit 2	closed	Ethernet mode selection bit 2 pulled low	
J15	open	Flash write enabled	closed	Flash write protected	*6.4*
J21	2 + 3	Voltage supervisor 2.5V monitoring enabled (for USB)	1 + 2[2]	Voltage supervisor 2.5V monitoring disabled	*4.2.1*
J22	1 + 2[3]	Voltage supervisor 1.2V monitoring disabled	2 + 3	Voltage supervisor 1.2V monitoring enabled (for FPGA)	*4.2.2*
J23	2 + 3	PF4 controls /AMS3 signal routing	1 + 2 2 + 4	/AMS3 always routed to USB & FPGA /AMS3 routing controlled by external signal AMS3_CTRL	*6.3.1*
J25	2 + 3	EEPROM U10 address bit A0 = 0	1 + 2	EEPROM U10 address bit A0 = 1	*6.5.1*
J26	2 + 3	EEPROM U10 address bit A1 = 0	1 + 2	EEPROM U10 address bit A1 = 1	
J27	2 + 3	EEPROM U10 address bit A2 = 0	1 + 2	EEPROM U10 address bit A2 = 1	

1 : See SMSC LAN8700I datasheet for strapping options. These bits control the PHY operating mode. Default jumper settings result in *All Capable. Auto-negotiation enabled.*

2 : This setting should only be used if the USB circuitry is unpopulated.

3 : This setting should only be used if the FPGA circuitry is unpopulated.

J34	1 + 2	FPGA bank 1 I/O voltage set to 3.3V	2 + 3	FPGA bank 1 I/O voltage provided via external supply signal FPGA_VCCIO	*11.2*
J35	1 + 2	FPGA bank 4 I/O voltage set to 3.3V	2 + 3	FPGA bank 4 I/O voltage provided via external supply signal FPGA_VCCIO	
J36	1 + 2	FPGA bank 3 I/O voltage set to 3.3V	2 + 3	FPGA bank 3 I/O voltage provided via external supply signal FPGA_VCCIO	
J43	1 + 2	FPGA programming mode set to *AS mode 20MHz*	2 + 3	FPGA programming mode set to *PS mode*	*11.1*
J45[1]	1 + 2	Ethernet PHY U4 address bit PHYAD0 = 1	2 + 3	Ethernet PHY U4 address bit PHYAD0 = 0	*7.2.2*
J46[1]	2 + 3	Ethernet PHY U4 address bit PHYAD1 = 0	1 + 2	Ethernet PHY U4 address bit PHYAD1 = 1	
J47[1]	2 + 3	Ethernet PHY U4 address bit PHYAD2 = 0	1 + 2	Ethernet PHY U4 address bit PHYAD2 = 1	
J48[1]	2 + 3	Ethernet PHY U4 address bit PHYAD3 = 0	1 + 2	Ethernet PHY U4 address bit PHYAD3 = 1	
J49[1]	2 + 3	Ethernet PHY U4 address bit PHYAD4 = 0	1 + 2	Ethernet PHY U4 address bit PHYAD4 = 1	

3.1 CLKOUT JUMPER J3

Jumper J3 is provided to route the buffered 25MHz processor clock signal CLKBUF to the phyCORE-connector for external use. By default this jumper is open, disconnecting CLKOUT from CLKBUF, resulting an inactive CLKOUT signal at the phyCORE-connector pin X1B1. To enable the CLKOUT signal place a 0-Ohm jumper at J3 to close it.

[1] : Use 10kOhm SMD resistor.

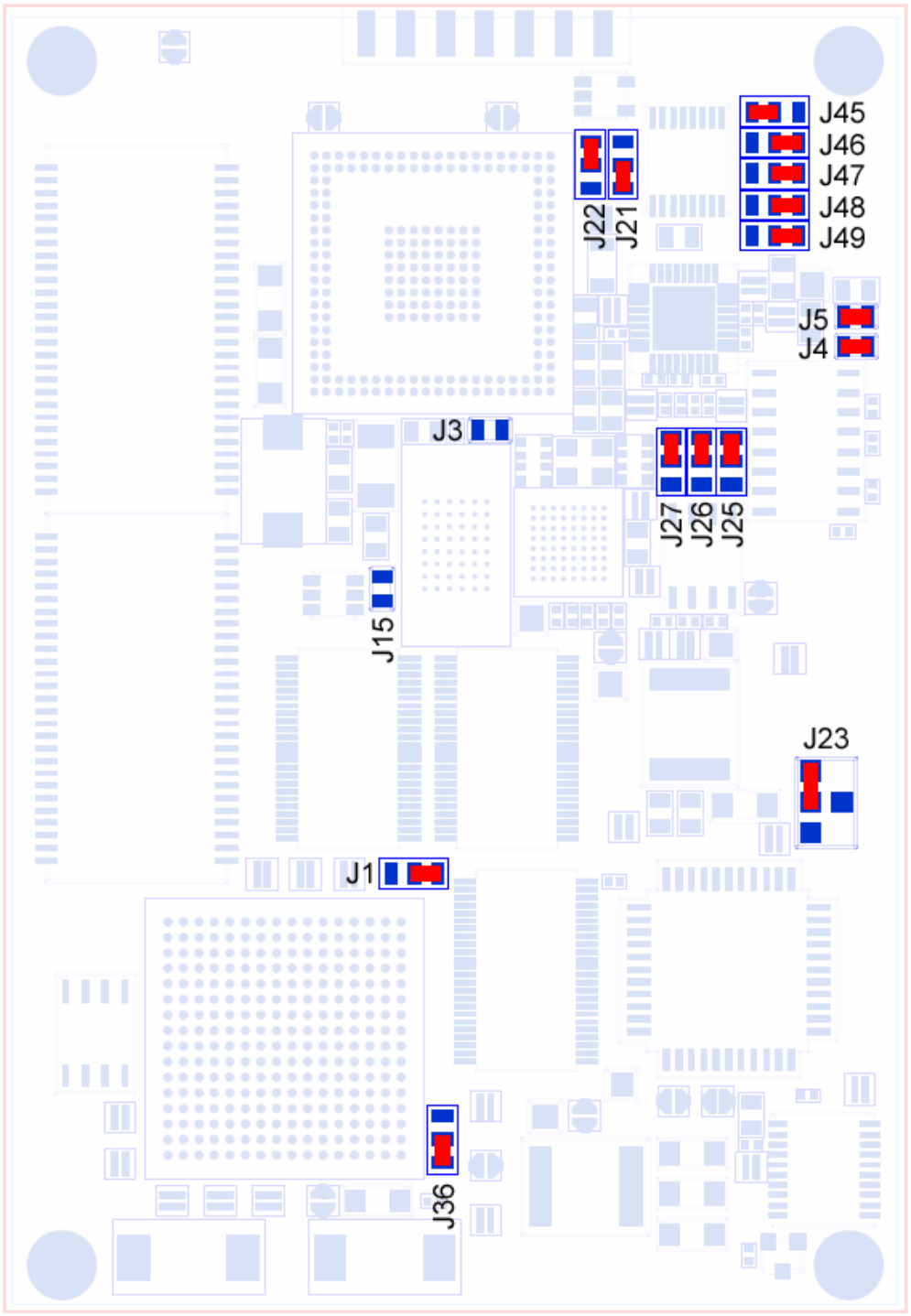

Figure 7: Default Jumper Settings on the phyCORE-BF537 (Top Side)

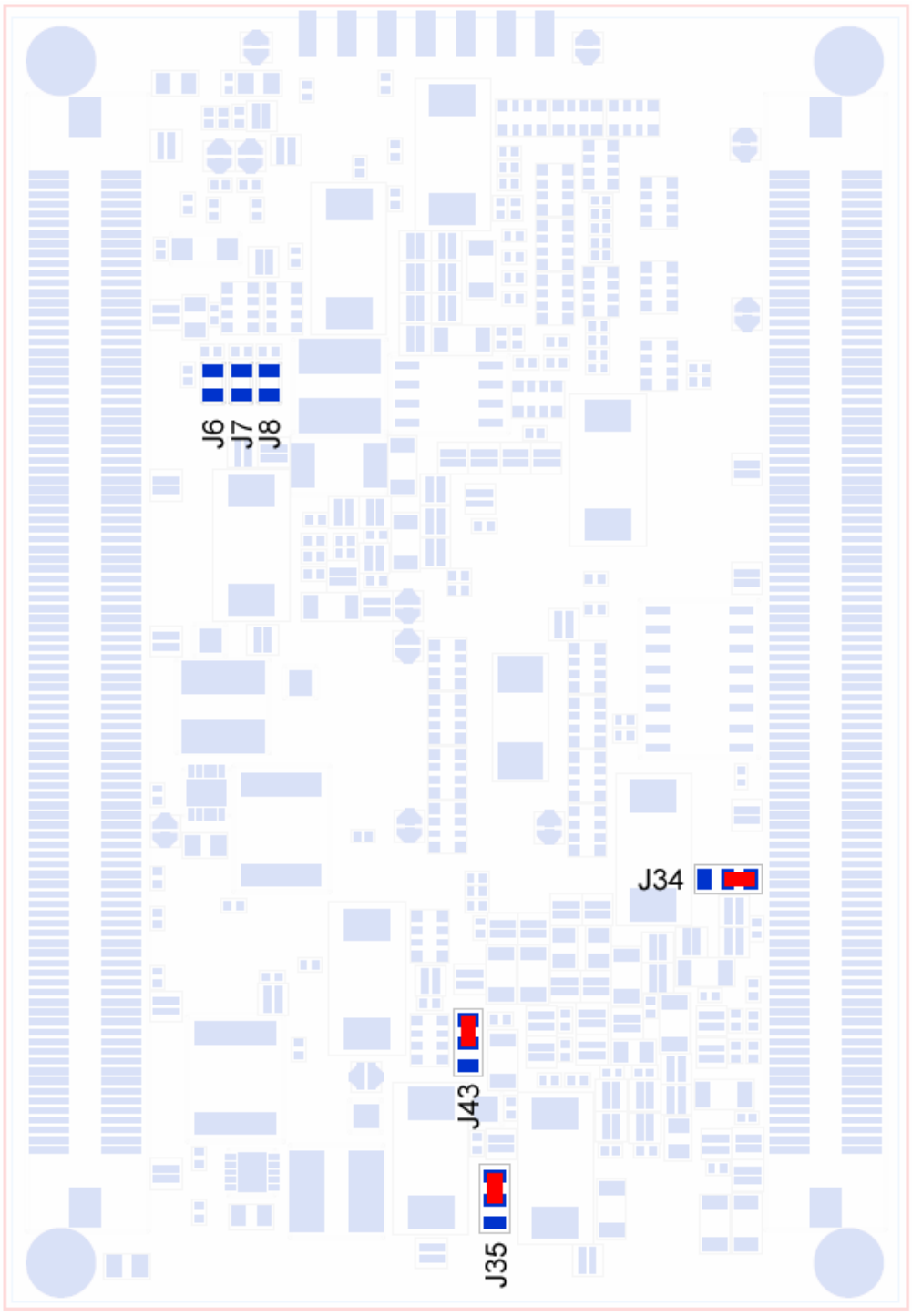

Figure 8: Default Jumper Settings on the phyCORE-BF537 (Bottom Side)

4 POWER REQUIREMENTS

The phyCORE-BF537 operates off a single voltage supply with a nominal value of 3.3V. On-board switching regulators generate the 2.5V, and 1.2V voltage supplies required by the BF537 DSP/MCU and on-board components from the primary 3.3V supplied to the module.

For proper operation the phyCORE-BF537 must be supplied with a single voltage source of 3.3V ± 0.1V allowing a current draw of at least 500 mA.

See *Table 1* from *section 2* above for applicable VCC power pins on the phyCORE-connector.

Caution:
Connect all +3.3V VCC input pins to your power supply and at least the matching number of GND pins neighboring the +3.3V pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

4.1 REAL TIME CLOCK

The connection of a battery is not essential to the functioning of the phyCORE-BF537. The battery, interfaced as voltage supply signal VBAT through X1C6 on the phyCORE-connector, provides power to the BF537's on-chip Real Time Clock (RTC). This offers a means of time keeping in the absence of power at the VCC pins while drawing minimal power from an external battery. When the phyCORE-BF537 is powered via VCC the RTC power domain automatically draws from the VCC supply. Switching from VCC to VBAT supply source occurs automatically when VCC is removed.

The VBAT input operating limits are listed in Table 3 below.

Table 3: VBAT Operating Limits

	MIN	MAX	UNITS
VBAT	2.25	3.6	V

It should be noted that although the maximum input voltage for VBAT is 3.6V, VBAT must remain less than VCC for the RTC to draw from VCC when it is present, otherwise if VBAT > VCC, the RTC will always be powered from VBAT. PHYTEC recommends an external battery with a nominal value of 3.0V.

Caution:
Operation beyond $VBAT_{max}$ could cause damage to the on-board components.

See section 13 Technical Specifications for battery power consumption.

4.2 VOLTAGE SUPERVISION (U2)

The phyCORE-BF537 comes equipped with a triple voltage supervisor IC located at U2. This voltage supervisor is responsible for monitoring the 3.3V supplied to the module through the phyCORE-connector as well as the 2.5V and 1.2V fixed supplies generated on the module. In the event any of these three supplies dip below permissible thresholds, the supervisor IC will hold the system /RESET line low until the supply voltages have returned to permissible operating levels and continue to hold the /RESET line low for another 216ms[1] afterwards. This ensures a typical reset duration of 216ms once the supply voltages have stabilized.

In addition to voltage supervisor, the supervisor IC also provides watchdog functionality. The watchdog provides an additional safety mechanism to prevent processor hangs by monitoring processor activity and resetting the processor if activity has ceased for a period of time.

On the phyCORE-BF537 the WDI input signal at phyCORE-connector pin X1D8 serves as the notification signal to the watchdog circuit that the processor is still active. Before the watchdog timeout period expires the processor should change the state of the WDI pin to reset the watchdog timer. In a typical configuration one of the ADSP-BF537 programmable flag pins (functioning as a GPIO) would be connected to the WDI signal and toggled from HIGH to LOW, or LOW to HIGH (a state change on the pin must occur, H->L or L->H is unimportant) at a rate shorter than the watchdog timeout period.

By default the watchdog circuit is enabled and the timeout period is set to ~940ms by capacitor C25. The processor should toggle the WDI signal before this timeout period expires, and should continue to toggle at a periodic interval less than the watchdog timeout period of 940ms to prevent a processor reset. In the event the processor hangs and is unable to recover the WDI signal will go untoggled by the processor, the watchdog timeout period will expire, and the watchdog circuit will assert the /RESET signal to the processor, resetting the system to a known state.

4.2.1 USB 2.5V SUPPLY MONITORING (J21)

Jumper J21 controls enabling and disabling the supervisor monitoring of the USB 2.5V supply voltage. By default this jumper is set to 2+3 and monitors the on-board 2.5V supply. This jumpers should only be set to 1+2 to disable 2.5V monitoring if the USB circuitry is not populating the module. This jumper will default to 2+3 if the module configuration excludes the USB circuitry and 2.5V supply. A customer should not have to modify this jumper.

4.2.2 FPGA 1.2V SUPPLY MONITORING (J22)

Jumper J22 controls enabling and disabling the supervisor monitoring of the FPGA 1.2V supply voltage. By default this jumper is set to 1+2 and the 1.2V supply is not monitored. Standard module configurations do not include the FPGA or the 1.2V supply regulator, requiring the 1.2V supervisor monitoring to be disabled. This jumper should only be set to 2+3 when the FPGA circuitry populates the module. This jumper will default to 2+3 if the module configuration includes the FPGA circuitry and 1.2V supply. You should not have to modify this jumper.

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[1]: Typical reset duration for populated reset timing capacitor C24. See LTC2901 datasheet for specifics.

5 SYSTEM CONFIGURATION

For operation of the phyCORE-BF537 several parts of the system should be initialized. Although very little initialization needs to take place for the most basic operation, it is typical that the following interfaces need to be initialized:

1. Core clock (cclk) and EBIU frequency (sclk)
2. SDRAM (operates from sclk)

Core Clock and External Memory Bus Interface Frequency
After a reboot the processor core clock is operating off of the main 25.0 MHz system crystal with a default PLL multiplication of 10x resulting in a core clock frequency of 250MHz. Most likely at some point the need for full processor frequency will arise. To initialize the core clock (cclk) and EBIU clock (sclk) a write to the following registers must occur:

1. PLL_DIV
2. PLL_CTL

Please refer to the *Dynamic Power Management* chapter of the ADSP-BF537 Hardware Reference Manual for details on setting these registers.

SDRAM
After a reboot the SDRAM interface is reset and must be initialized. The initialization procedure involves initializing two primary interfaces: 1) the BF537 SDRAM controller, and 2) the SDRAM itself. Initialization of the BF537 SDRAM controller sets up the processor with the proper timing and size configuration values required to interfaces the external SDRAM. The initialization of the SDRAM sets up the "mode" and "extended mode" registers on the SDRAM with information such as burst length, burst type, CAS latency, driver strength, etc... The BF537 SDRAM controller handles step (2) above. SDRAM configuration is accomplished through writes to the following registers:

1. EBIU_SDRRC
2. EBIU_SDBCTL
3. EBIU_SDGCTL

5.1 BOOT PROCESS

By default the phyCORE-BF537 is configured to boot from the on-board external 16-bit NOR Flash device populated at U5. After a reset the processor begins executing the boot kernel residing in the on-chip boot ROM located at 0xEF00 0000. The boot kernel is responsible for copying application data into memory for execution, along with executing initialization code required to complete the boot process.

The boot kernel begins by reading a well defined stream of data called the boot stream from the Flash memory at address 0x2000 0000. The boot stream consists of a number of data block/10-Byte header pairs that instruct the boot kernel on how to process the Flash data. Each block of data will either (1) be copied into internal or external memory, or (2) be copied into internal memory and executed as an initialization block. After the boot stream has been processed the boot kernel jumps to the reset vector stored in the EVT1 register which is set to 0xFFA0 0000 (start of instruction SRAM) by the boot kernel after a hardware reset.

A detailed explanation of the boot process can be found in the *System Reset and Booting* chapter of the ADSP-BF537 Hardware Reference Manual.

A typical application will probably contain at least one init block in the boot stream which will at the very least initialize SDRAM for application code. Note that this init block must be executed prior to specifying SDRAM as a target address for application code further down the boot stream. Beyond SDRAM initialization an init block can also be used to initialize the processor clocks, along with EBIU initialization for faster booting. Note that after a hardware reset the EBIU bus frequency is 50MHz with 15 read access cycles, 3 hold cycles, 4 setup cycles and 4 bank memory transition cycles. For faster booting the bus frequency should be increased and the bank timing parameters should be set to maximize the read frequency to the Flash. To adjust the external memory bank timing parameters the following registers must be written:

1. EBIU_AMGCTL
2. EBIU_AMBCTL0
3. EBIU_AMBCTL1

5.2 BOOT MODES

The phyCORE-BF537 supports all 7 processor booting modes. The boot mode is controlled by strapping the BMODE0, BMODE1, an BMODE2 pins HIGH or LOW during the boot process. The boot mode pins are available at the phyCORE-connector pins X1D41, X1D42, X1D43. Table 4 below summarizes the available boot modes, along with the default phyCORE-BF537 boot mode.

Table 4: Boot Mode Configuration Settings

BMODE2..0 CONFIGURATION	BOOT MODE
000	Boot directly from external Flash populated at U5 (bypass boot ROM)
001*	Boot from external Flash at U5 using the on-chip boot ROM
010	Reserved
011	Boot from external off-module SPI memory device
100	Boot from external SPI host
101	Boot from internal on-module or external off-module TWI (I²C) memory device
110	Boot from external TWI (I²C) host
111	Boot from external UART host

*= Default Setting

To use a different boot mode (other than the default) the BMODE0,1,2 signals at the phyCORE-connector pins X1D41,42,43 should be connected directly to either VCC (3.3V) or GND. The phyCORE-BF537 straps these signals with 10k pull-up and pull-down resistors on the module. An external pull-up or pull-down resistor is not recommended.

Note that all processor boot modes except boot mode “000” use the on-chip boot ROM. If boot mode “000” is required it is the customer's task to write the necessary boot loader in order to replace on the boot ROM boot kernel for system booting.

6 System Memory

The phyCORE-BF537 provides three types of on-board memory:

- SDR SDRAM (U8/U9): from 16MB to 128MB
- NOR FLASH (U5): from 1MB to 4MB
- EEPROM (U10): from 1KB to 32KB

6.1 Memory Model

The phyCORE-BF537 memory map is summarized in Table 5 below.

Table 5: phyCORE-BF537 Memory Map

Address – Size	Function	Comments
0xFFE0 0000 – 2MB	Core MMR Registers	
0xFFC0 0000 – 2MB	System MMR Registers	
0xFFB0 1000 – N/A	Reserved	
0xFFB0 0000 – 4KB	Scratchpad SRAM	
0xFFA1 4000 – N/A	Reserved	
0xFFA1 0000 – 16KB	Instruction SRAM/CACHE	
0xFFA0 C000 – N/A	Reserved	
0xFFA0 8000 – 32KB	Instruction Bank B SRAM	
0xFFA0 0000 – 32KB	Instruction Bank A SRAM	
0xFF90 8000 – N/A	Reserved	
0xFF90 4000 – 16KB	Data Bank B SRAM/CACHE	
0xFF90 0000 – 16KB	Data Bank B SRAM	
0xFF80 8000 – N/A	Reserved	
0xFF80 4000 – 16KB	Data Bank A SRAM/CACHE	
0xFF80 0000 – 16KB	Data Bank A SRAM	
0xEF00 0800 – N/A	Reserved	
0xEF00 0000 – 2KB	Boot ROM	
0x2040 0000 – N/A	Reserved	

ADDRESS – SIZE	FUNCTION	COMMENTS
0x2030 0000 – 1MB	ASYNC Bank 3	Shared between Flash @ U5, USB @ U11, and FPGA @ U28; see section 6.3 for a detailed explanation
0x2020 0000 – 1MB	ASYNC Bank 2	Maps to Flash if at least 4MB are populated at U5, otherwise free for external use
0x2010 0000 – 1MB	ASYNC Bank 1	Maps to Flash if at least 2MB are populated at U5, otherwise free for external use
0x2000 0000 – 1MB	ASYNC Bank 0	Always maps to Flash @ U5
0x0000 0000 – 512MB	External SDRAM (U8 & U9)	Limited to 128MB max. on phyCORE-BF537

6.2 SDR SDRAM (U8, U9)

The phyCORE-BF537 comes preconfigured with 16, 32, 64 or 128MB of 133MHz SDR SDRAM configured for 16-bit access using two 8-bit wide DRAM chips at U8 and U9.

The ADSP-BF537 is capable of addressing a single RAM bank located at memory address 0x0000 0000 and extending to 0x1FFF FFFF. It should be noted that this is beyond what the phyCORE-BF537 supplies for on-board memory. *Refer to Table 6* for permissible SDRAM memory access ranges.

Table 6: Valid SDRAM Memory Address Ranges

SDRAM SIZE	LOWER MEMORY ADDRESS	UPPER MEMORY ADDRESS
16MB	0x0000 0000	0x00FF FFFF
32MB		0x01FF FFFF
64MB		0x03FF FFFF
128MB		0x07FF FFFF

6.3 EXTERNAL MEMORY BUS MAPPING

The ADSP-BF537 provides 4MB of asynchronous external memory space for memory mapped peripherals using 19 address signals and four chip selects on a 16 bit data bus. The 4MB of external memory space are divided up into 4 external banks known as Asynchronous Memory banks 0, 1, 2, and 3. Each external memory bank has a dedicated memory select signal called an Asynchronous Memory Select signal, identified as /AMS0, 1, 2, and 3 respectively. All four memory select signals are active low.

The phyCORE-BF537 shares the external memory bus between Flash, the USB controller, and an FPGA. To accommodate various Flash density population options and USB/FPGA populate/ depopulate options a CPLD populated at U6 is responsible for chip select decoding. The CPLD (EPM7032) uses the input signals in Table 7 to decode and generate the output signals in Table 8.

Table 7: CPLD Decode Input Signals

SIGNAL NAME	DESCRIPTION
/AMS3	Processor **A**synchronous **M**emory **S**elect signal 3. Used for Flash upper address bit generation, Flash chip select, USB chip select, and FPGA chip select generation.
/AMS2	Processor **A**synchronous **M**emory **S**elect signal 2. Used for Flash upper address bit generation.
/AMS1	Processor **A**synchronous **M**emory **S**elect signal 1. Used for Flash upper address bit generation.
/AMS0	Processor **A**synchronous **M**emory **S**elect signal 0. Used for Flash upper address bit generation.
PLD_IO17	Asynchronous bank 3 chip select generation input. Used to tell the CPLD to either generate the /FLASH_CS for asynchronous bank 3 accesses, or to split the bank and generate /USB_CS and /FPGA_CS for asynchronous bank 3 accesses.
A19	Processor memory bus address bit 19. Used to split asynchronous bank 3 between FPGA & USB.
A18	Processor memory bus address bit 18. Used to split asynchronous bank 3 between FPGA & USB.
A17	Processor memory bus address bit 17. Used to split asynchronous bank 3 between FPGA & USB.
A16	Processor memory bus address bit 16. Used to split asynchronous bank 3 between FPGA & USB.
A15	Processor memory bus address bit 15. Used to split asynchronous bank 3 between FPGA & USB.
A14	Processor memory bus address bit 14. Used to split asynchronous bank 3 between FPGA & USB.
/AOE	Processor memory bus **A**synchronous **O**utput **E**nable signal. Used to generate buffer output enable signal /BUF_OE.
/AWE	Processor memory bus **A**synchronous **W**rite **E**nable signal. Currently not used in CPLD firmware. Routed to CPLD for customer flexibility.
/ARE	Processor memory bus **A**synchronous **R**ead **E**nable signal. Currently not used in CPLD firmware. Routed to CPLD for customer flexibility.
/RESET	System reset signal from the voltage supervisor. Currently not used in the CPLD firmware. Routed to CPLD for customer flexibility.

Table 8: CPLD Decode Output Signals

SIGNAL NAME	DESCRIPTION
FLASH_A20	Flash upper address bit A20 generated from /AMS3..0
FLASH_A21	Flash upper address bit A21 generated from /AMS3..0
/FLASH_CS	Flash chip select signal generated from PLD_IO17 and /AMS3
/USB_CS	USB chip select signal generated from PLD_IO17, /AMS3, and A19..14.
/FPGA_CS	FPGA chip select signal generated from PLD_IO17, /AMS3, and A19..14.
BUF_DIR	Buffer direction signal generated from /AOE
/BUF_OE	Buffer output enable signal. Current firmware keeps this at “0”.

The /FLASH_CS signal is always asserted when /AMS0, 1, or 2 are asserted. Whether or not /FLASH_CS is asserted at the time /AMS3 is asserted is dependent upon the PLD_IO17 input signal to the CPLD.

The PLD_IO17 input signal tells the CPLD to either use ASYNC bank 3 for Flash, or to split the bank between the USB and FPGA. If PLD_IO17 = “1” then the CPLD will assert /FLASH_CS when ASYNC bank 3 is accessed. If PLD_IO17 = “0” then the CPLD will assert the /FPGA_CS or /USB_CS, when ASYNC bank 3 is accessed; /USB_CS is asserted if A14..19 < 0x40, and /FPGA_CS is asserted if A14..19 >= 0x40. In this manner the asynchronous memory bank 3 is shared between the Flash, USB, and FPGA.

In the default configuration J23 connects programmable flag PF4 from the ADSP-BF537 to the PLD_IO17 input control signal. After a hardware reset PF4 will be default configured as an input and R32 will pull PLD_IO17 to “1” defaulting ASYNC bank 3 access to Flash. After booting has completed and code has been loaded from Flash, the user application should configure the PF4 signal as an output and drive it to “0”, thereby configuring ASYNC bank 3 to be shared between the USB and FPGA.

When PLD_IO17 = “0” the memory mapping of ASYNC bank 3 is in accordance with Table 9.

Table 9: ASYNC Bank 3 Memory Map when USB/FPGA are Selected

ADDRESS RANGE	SIGNAL	SIZE
0x2030 0000 – 0x2030 3FFF	/USB_CS	16KB
0x2030 4000 – 0x203F FFFF	/FPGA_CS	1008KB

The FLASH_A20 and FLASH_A21 signals are generated from /AMS3..0; PLD_IO17 does not affect the FLASH_A20/21 signals.

/BUF_OE is permanently set to “0”, enabling the bus buffers. There are no logic decisions to generate this signal.

BUF_DIR follows the /AOE with the current CPLD firmware. In standard configurations the BUF_DIR signal is not used, and instead jumper J1 connects /AOE directly to the buffer direction control pin.

It should be noted that EPM7032 device populating the phyCORE-BF537 has a 10ns speed grade. The maximum propagation delay from input to output is equal to the 10ns speed grade. When doing timing analysis on CPLD generated signals this extra maximum delay should be taken into consideration.

The on-board CPLD at U6 is reprogrammable via the CPLD JTAG pins available at the phyCORE-connector pins X1C78, X1C79, X1C80 and X1C81. This provides the capability to partition the external memory banks for a custom configuration if the default configuration does not meet user needs. Additional PLD signals are also made available at the phyCORE-connector and are prefixed with "PLD_" in the signal name. Additional chip selects for external memory mapped peripherals can be generated, such as splitting ASYNC bank 2 to share between two memory mapped devices external to the phyCORE-BF537.

6.3.1 PLD_IO17 Control Source (J23)

The driving source for PLD_IO17 is controlled by J23. By default processor signal PF4 is connected to PLD_IO17. Alternatively PLD_IO17 can be controlled by the external signal AMS3_CTRL if PF4 is needed for other operations. PLD_IO17 can also be configured to permanently select Flash, or configured to permanently select the USB/FPGA. Table 10 below summarizes the configuration options for PLD_IO17 using J23.

Table 10: PLD_IO17 Control Source Options via J23

Description	J23
PLD_IO17 = "0"; ASYNC bank 3 permanently split between USB and FPGA	1 + 2
PLD_IO17 controlled by processor signal PF4	2 + 3
PLD_IO17 controlled by AMS3_CTRL	2 + 4
PLD_IO17 = "1"; ASYNC Bank 3 permanently accesses Flash	unplaced

6.4 Flash Memory (U5)

Use of Flash as non-volatile memory on the phyCORE-BF537 provides an easily reprogrammable means of code storage. Flash memory is accessed via the external memory bus interface (EBIU) as a memory mapped peripheral. The phyCORE-BF537 is capable of supplying 1, 2 or 4MB of external on-board Flash. Valid Flash memory address ranges are summarized in Table 11 below.

Table 11: Valid Flash Memory Address Ranges

Size	Lower Memory Address	Upper Memory Address
1MB	0x2000 0000	0x200F FFFF
2MB		0x201F FFFF
4MB		0x203F FFFF

These Flash devices are programmable with 3.3V. No dedicated programming voltage is required.

Refer to section 6.3.1 for explanation of chip select and address decode generation when using 4MB of Flash.

6.5 EEPROM (U10)

The phyCORE-BF537 is populated with a Microchip 24FC256[1] non-volatile 32KB EEPROM (U10) with an TWI (I²C) interface to store configuration data or other general purpose data. This device is accessed through the TWI port on the ADSP-BF537. The serial clock signal and serial data signal for the TWI port are made available at the phyCORE-connector as I2C_SDA on X1D32 and I2C_SCL on X1C31. In addition the write protect signal of the EEPROM is also made available at the phyCORE-connector as signal I2C_WP on pin X1D31. By default the on-board pull-down resistor R17 will not provide protection of the EEPROM, allowing writes to the device. To protect the EEPROM from writes the I2C_WP signal should be connected directly to 3.3V external to the module.

Three solder jumpers are provided to set the lower address bits: J25, J26, and J27. *Refer to section 6.5.1 for details on setting these jumpers.*

6.5.1 Setting the EEPROM Lower Address bits (J25, J26, J27)

The optional 32KB I²C EEPROM populating U10 on the phyCORE-BF537 has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see Microchip 24FC256 data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J25, J26 and J27. J25 sets address bit A0, J26 address bit A1, and J27 address bit A2. *Table 12* below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

The following configurations are possible:

Table 12: J27, J26, J25 EEPROM Lower Address Bits

I²C Device Address	J27	J26	J25
1010 000*	2 + 3*	2 + 3*	2 + 3*
1010 001	2 + 3	2 + 3	1 + 2
1010 010	2 + 3	1 + 2	2 + 3
1010 011	2 + 3	1 + 2	1 + 2
1010 100	1 + 2	2 + 3	2 + 3
1010 101	1 + 2	2 + 3	1 + 2
1010 110	1 + 2	1 + 2	2 + 3
1010 111	1 + 2	1 + 2	1 + 2

* = Default setting

1: See the manufacturer's data sheet for interfacing and operation details.

7 SERIAL INTERFACES

7.1 RS-232 TRANSCEIVER (U3)

A MAX3232 RS232 transceiver supporting typical data rates of 235kbps populates the phyCORE-BF537 at U3. This device converts the signal levels for:

- UART0_RX / UART0_TX
- UART1_RX / UART1_TX

All RS-232 interfaces enable connection of the module to a COM port on a host-PC. In this instance the RxD line of the transceiver is connected to the TxD line of the COM port; while the TxD line is connected to the RxD line of the COM port. The ground potential of the phyCORE-BF537 circuitry needs to be connected to the applicable ground pin on the COM port as well.

7.1.1 UART RS-232/TTL LEVEL SELECTION (J4, J5)

In may be necessary or desired to use one, or both UARTs at TTL levels. For this purpose jumpers J4 and J5 allow disconnection of the receive signals from the RS-232 transceiver at U3. In the normal configuration J4 and J5 are closed and U3 drives the UART receive signals to the ADSP-BF537. To use the UART interfaces at TTL levels J4 or J5 must be removed (depending on which UART interface is needed at TTL level) to prevent multiple sources from driving the ADSP-BF537 UART Rx signals simultaneously. Refer to Table 13 and Table 14 below for a summary of the J4, J5 jumper settings required to use the UARTs at RS-232 or TTL levels.

Table 13: UART0 RS-232/TTL Level Selection

DESCRIPTION	J4
UART0_RX to the processor is driven by the RS-232 transceiver at U3; UART0 is interfaced at RS-232 levels using UART0_RX_RS232 at X1D22 and UART0_TX_RS232 at X1D23	closed*
UART0_RX is disconnected from the RS-232 transceiver at U3; UART0 is interfaced at TTL levels using UART0_RX at X1D16 and UART0_TX at X1D17	open

* = Default

Table 14: UART1 RS-232/TTL Level Selection

DESCRIPTION	J5
UART1_RX to the processor is driven by the RS-232 transceiver at U3; UART1 is interfaced at RS-232 levels using UART1_RX_RS232 at X1C21 and UART1_TX_RS232 at X1C23	closed*
UART1_RX is disconnected from the RS-232 transceiver at U3; UART1 is interfaced at TTL levels using UART1_RX at X1C19 and UART1_TX at X1C20	open

* = Default

7.2 ETHERNET (U4)

The phyCORE-BF537 comes populated with an SMSC LAN8700I Ethernet PHY at U4 supporting 10/100 MBit/s Ethernet connectivity. The PHY uses an MII interface to the Ethernet MAC integrated on the ADSP-BF537.

The LAN8700I supports the HP Auto-MDIX function eliminating the need for consideration of a direct connect LAN cable, or a cross-over patch cable. The LAN8700I detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly.

Interfacing the Ethernet port involves adding an RJ45 and appropriate magnetic devices in your design. Please consult the phyCORE-BF537 Carrier Board schematics as a reference.

7.2.1 CONFIGURING THE PHY OPERATING MODE (J6, J7, J8)

The LAN8700I operating mode is set via solder jumpers J6, J7, and J8. By default the PHY operating mode is set to *All capable. Auto-negotiation enabled.* If a different operating mode is required J6, J7, and J8 can be set according to Table 15 below. J6 sets MODE0, J7 sets MODE1, and J8 sets MODE2. By default these signals are driven to "1" via weak internal pull-up resistors on the PHY. To set a mode bit to "0" the corresponding jumper should be closed with a 0-Ohm resistor. Refer to the SMSC LAN8700I datasheet for a detailed presentation of the PHY operating modes.

Table 15: Ethernet PHY Operating Mode Selection[1]

MODE[2:0]	J8	J7	J6	DESCRIPTION
000	closed	closed	closed	10Base-T Half Duplex. Auto-negotiation disabled.
001	closed	closed	open	10Base-T Full Duplex. Auto-negotiation disabled.
010	closed	open	closed	100Base-TX Half Duplex. Auto-negotiation disabled. CRS is active during Transmit & Receive.
011	closed	open	open	100Base-TX Full Duplex. Auto-negotiation disabled. CRS is active during Receive.
100	open	closed	closed	100Base-TX Half Duplex is advertised. Auto-negotiation enabled. CRS is active during Transmit & Receive.
101	open	closed	open	Repeater mode. Auto-negotiation enabled. 100Base-TX Half Duplex is advertised. CRS is active during Receive.
110	open	open	closed	Power Down mode. In this mode the PHY wake-up in Power-Down mode.
111*	open	open	open	All capable. Auto-negotiation enabled.

* = Default

1 : Table copied from SMSC LAN8700I datasheet, rev. 0.6, page 52, Table 5.45.

7.2.2 CONFIGURING THE PHY ADDRESS (J45, J46, J47, J48, J49)

Solder jumpers J45 through J49 control setting the Ethernet PHY address. By default the PHY address is set to 00001b with J45 = 1+2, J46-J49 = 2+3. J45 sets PHYAD0, J46 sets PHYAD1, J47 sets PHYAD2, J48 sets PHYAD3, and J49 sets PHYAD4. Jumpers J45-49 are two position jumpers, either set to 1+2 or 2+3 via 10k resistors. A 1+2 setting corresponds to a “1” for the designated PHY address bit, while a 2+3 corresponds to a “0”.

7.3 USB DEVICE CONTROLLER (U11)

The phyCORE-BF537 comes populated with a PLX NET2272 USB device controller supporting full-speed (12Mbps) and high-speed (480Mbps) data rates at U11. The NET2272 is interfaced to the ADSP-BF537 as a memory mapped peripheral on asynchronous memory bank 3.

A detailed discussion of the memory bus mapping to access the USB is presented in section 6.3. In short the USB address space is limited to: 0x2030 0000 – 0x2030 3FFF. Although 16KB of address space has been allotted to the USB controller, only memory spaces from 0x2030 0000 – 0x2030 007C is used by the USB, with address bits A1 and A0 being “don’t care”.

The USB controller provides 5 address bits, which have been connected to A2..A6 of the processor. Access to the USB registers is done using the (1) *Non-Multiplexed Direct Address Mode* and (2) *Non-Multiplexed Indirect Address Mode* of the USB controller. In mode (1) the first 32 USB registers are directly accessible by providing address information on A2..A6. In mode (2) the USB registers beyond the first 32 (corresponding to 0x2030 007C as the last register of the first 32) are accessed with the address pointer and data registers located at 0x2030 0000 and 0x2030 0004. An example of accessing the registers is provided below:

Reading/Writing to the Scratch Pad register SCRATCH located at 0x1d:

1) This is within the first 32 registers, so addressing mode (1) from above is used
    a. Shift the register address left by 2; 0x1d << 2 becomes 0x74
    b. Add the shifted address to the USB base address 0x2030 0000
    c. Perform read or write access to the resulting location; in this case 0x2030 0074

Reading/Writing to the Local Bus Control register LOCCTL located at 0x22:

2) This is beyond the first 32 registers, so addressing mode (2) from above is used
    a. Write the address of the desired register to the REGADDRPTR register of the USB controller located at 0x2030 0000; in this case 0x22 is written
    b. Read or Write the data from the REGDATA register of the USB controller located at 0x2030 0004

Interfacing the USB controller involves adding a USB Standard B connector to the target application design. The phyCORE-BF537 Carrier Board reference schematics should be consulted for a proper implementation. Careful layout of the USB data lines should be handled, in particular routing the USB_DM and USB_DP signals as a controlled impedance 90-Ohm differential pair is critical to the proper operation of the USB interface at high-speed data rates.

8 ANALOG-TO-DIGITAL CONVERTER (U17)

To extend the functionality of the ADSP-BF537, the phyCORE-BF537 incorporates an Analog Devices AD7927 12-bit, 8 channel, 200ksps analog-to-digital converter populated at U17. The ADC is interfaced to the ADSP-BF537 via the SPI port using SPI slave select signal 5 of the processor.

The analog input signal range of the 8 input channels (ADC_IN0..8) is adjustable between two ranges. In the default REF_IN operating mode the input range is from 0V to 2.5V. In the REF_IN*2 operating mode the input range is extended up to 5V. When operating in the 2X operating mode the operating voltage of the ADC must be between 4.75V and 5.25V. The ADC operating voltage is supplied via the ADC_AVCC power input pin available at phyCORE-connector pins X1C4 and X1C5. Table 16 below summarizes the required ADC_AVCC input voltage for the given mode, along with the permissible analog input ranges in that mode.

Table 16: ADC Mode Setting Summary

REQUIRED ADC_AVCC VOLTAGE	MODE	ANALOG INPUT RANGE
2.7 -- 5.25	REF_IN	0V to 2.5V
4.75 -- 5.25	REF_IN*2	0V to 5.0V

The signal ADC_AVCC has no connection to any supply voltage on the module, hence disabling the ADC. ADC_AVCC should be connected to a external source in the range specified in Table 16 for the desired mode of operation in your design.

9 CPLD (U6)

To give maximum flexibility for interfacing the external memory bus on the ADSP-BF537 an Altera EPM7032 CPLD device populated at U6 has been incorporated into the phyCORE-BF537. The EPM7032 is responsible for Flash, USB, and FPGA chip select generation, Flash memory upper address bit generation, and bus buffer output enable and direction control. Refer to section 6.3 for a detailed discussion of chip select and address bit generation. Refer to section 10 for a detailed discussion of bus buffer control.

In addition to the above, the remaining free CPLD I/O's can be used to further customize the address space on the external memory bus. An example showing how free CPLD I/O's can be used to customize the external memory address space is provided below:

A system requires 4MB of Flash, an SD Card controller, and a full functioning modem UART. In this scenario a phyCORE-BF537 with a 4MB Flash memory population and FPGA population could be used as the solution (USB depopulated). Both the SD Card controller and the modem UART would be implemented on the FPGA. With two functions implemented on the FPGA it would be beneficial to have two separate chip select signals to the FPGA to access each function. Using one of the freely available PLD I/O signals an extra chip select could be generated to further divide up asynchronous memory bank 3. The CPLD would examine the address bits A14..19, along with /AMS3 (Asynchronous Memory Select 3) to generate the /FPGA_CS and a new /FPGA_CS2 signal. When /AMS3 is asserted and 0x0 < A14…A19 <= 0x1F then /FPGA_CS is asserted. When /AMS3 is asserted and 0x1f < A14..A19 <= 0x3F then /FGPA_CS2 is asserted. In this manner asynchronous memory bank 3 is split with 0.5MB of address space going to /FPGA_CS (perhaps this is the SD Card controller), and 0.5MB of address space going to /FPGA_CS2 (perhaps this is the full functioning modem UART).

Table 17 below summarizes the input signals routed to the CPLD, Table 18 summarizes the output signals generated by the CPLD, and Table 19 summarizes the remaining free CPLD I/O for custom use.

Table 17: CPLD Input Signals from the Processor

SIGNAL NAME	SIGNAL DESCRIPTION
/AMS0	Processor Asynchronous Memory Bank 0 Select
/AMS1	Processor Asynchronous Memory Bank 1 Select
/AMS2	Processor Asynchronous Memory Bank 2 Select
/AMS3	Processor Asynchronous Memory Bank 3 Select
/AWE	Processor Asynchronous Write Enable
/ARE	Processor Asynchronous Read Enable
/AOE	Processor Asynchronous Output Enable
A14	Processor Address bus bit 14
A15	Processor Address bus bit 15
A16	Processor Address bus bit 16
A17	Processor Address bus bit 17
A18	Processor Address bus bit 18
A19	Processor Address bus bit 19
/RESET	Voltage supervisor /RESET output

Table 18: CPLD Output Signals

SIGNAL NAME	SIGNAL DESCRIPTION
BUF_DIR	Data Bus Buffer Direction Control
/BUF_OE	Data Bus Buffer Output Enable
/FPGA_CS	FPGA Chip Select
/USB_CS	USB Chip Select
/FLASH_CS	Flash Chip Select
FLASH_A20	Flash Address bit A20
FLASH_A21	Flash Address bit A21

Table 19: Free CPLD I/O Signals

SIGNAL NAME	SIGNAL DESCRIPTION
PLD_IO4/TDI	I/O #4 / JTAG TDI
PLD_IO9/TMS	I/O #9 / JTAG TMS
PLD_IO18	I/O #18
PLD_IO19	I/O #19
PLD_IO20/TDO	I/O #20 / JTAG TDO
PLD_IO21	I/O #21
PLD_IO22	I/O #22
PLD_IO23	I/O #23
PLD_IO24	I/O #24
PLD_IO25/TCK	I/O #25 / JTAG TCK
PLD_IO26	I/O #26
PLD_IO27	I/O #27
PLD_IO28	I/O #28
PLD_IO29	I/O #29

Reprogramming of the CPLD for customization can be done using the JTAG interface pins of the CPLD. These interface pins are accessed via the CPLD JTAG header X18 on the phyCORE-BF537 Carrier Board. PHYTEC recommends a *USB-Blaster Download Cable* available from Altera, along with the freely available Quartus II Web Edition software development environment from Altera. For more information visit http://www.altera.com. PHYTEC also provides the VHDL project used to program the CPLD for the standard phyCORE-BF537 configuration as a reference.

10 BUS BUFFERS (U12, U13, U24)

The phyCORE-BF537 provides a buffered version of the processor's external memory bus via bus buffers U12, U13, and U24. Buffer U12 provides the 16-bit buffered data bus, with both output enable and direction control via the CPLD and processor /AOE signal. Buffers U13 and U24 provide unidirectional buffered address bus and control signals.

The data bus buffer U12 defaults to using the processor /AOE signal to control buffer direction, but can be configured to use the BUF_DIR signal provided by the CPLD for custom needs via solder jumper J1. The buffer output enable is always controlled via the /BUF_OE provided by the CPLD. In the standard configuration /BUF_OE is always driven to "0" by the CPLD, permanently enabling the data bus buffer.

The buffers provide a means to connect external memory, or memory mapped peripherals to the ADSP-BF537 external memory bus.

11 ALTERA CYCLONE II FPGA (U28)

The phyCORE-BF537 provides an Altera Cyclone II FPGA populated at U28 to add additional functionality not found on the ADSP-BF537. Two different FPGA variants can populate the phyCORE-BF537:

- the EP2C5 supporting 4,608 logic elements, or
- the EP2C8 supporting 8,256 logic elements.

A variety of free IP cores are available from the Altera website. Altera also provides the Quartus II Web Edition development software free of charge to implement designs on the Cyclone II FPGA.

In addition to the software development environment provided by Altera, PHYTEC recommends a *USB-Blaster Download Cable* (or equivalent) interfaced through the FPGA's JTAG port for code development and testing. The USB-Blaster can be purchased from Altera.

The Cyclone II FPGA is interfaced to the ADSP-BF537 through the buffered external memory bus. Table 20 below shows the bus interface connection between the ADSP-BF537 and the FPGA. All processor bus signals connect to bank 2 of the FPGA.

Table 20: FPGA to Processor Memory Bus Connection

PROCESSOR SIGNAL	BUFFERED SIGNAL	FPGA PIN NUMBER
A1	BUF_A1	C12
A2	BUF_A2	C13
A3	BUF_A3	A10
A4	BUF_A4	B10
A5	BUF_A5	A14
A6	BUF_A6	B14
A7	BUF_A7	A13
A8	BUF_A8	B13
A9	BUF_A9	A12
A10	BUF_A10	B12
A11	BUF_A11	A11
A12	BUF_A12	B11
A13	BUF_A13	G11
A14	BUF_A14	G10
A15	BUF_A15	F9
A16	BUF_A16	F10
A17	BUF_A17	D10

A18	BUF_A18	D11
A19	BUF_A19	B9
/ABE0	/BUF_ABE0	A9
/ABE1	/BUF_ABE1	C11
D0	BUF_D0	A4
D1	BUF_D1	B4
D2	BUF_D2	B7
D3	BUF_D3	A7
D4	BUF_D4	F8
D5	BUF_D5	F7
D6	BUF_D6	A6
D7	BUF_D7	B6
D8	BUF_D8	G7
D9	BUF_D9	G6
D10	BUF_D10	C6
D11	BUF_D11	D6
D12	BUF_D12	C4
D13	BUF_D13	C5
D14	BUF_D14	A5
D15	BUF_D15	B5
/AOE	/BUF_AOE	A3
/ARE	/BUF_ARE	B3
/AWE	/BUF_AWE	E6
ARDY	BUF_ARDY	F6
N/A	/FPGA_CS	D8
N/A	/FPGA_RST	A8

Note that the /FPGA_RST signal and /FPGA_CS signal are not sourced directly from the processor.

The /FPGA_RST signal is the result of a logic AND combination of the on-board system /RESET signal, and two additional soft reset signals called /FPGA_RST0 and /FPGA_RST1. Both soft reset signals are available at the phyCORE-connector and provide a means for an alternative soft reset to the FPGA independent of the system /RESET signal generated by the voltage supervisor.

The /FPGA_CS signal is generated from the on-board CPLD by examining the upper memory bus address bits (A14..19), and the Asynchronous Memory Bank 3 Select signal (/AMS3). The resulting /FPGA_CS signal is mapped to the processor address range 0x2030 4000 – 0x203F FFFF (the upper 1008KB of asynchronous bank 3). Reads or writes to this memory space will assert the /FPGA_CS signal.

When calculating timing parameters for interfacing the FPGA additional considerations must be made beyond the timing waveforms in the BF537 Hardware Reference Manual for external memory bus timing. The delay through the CPLD and the delay through the bus buffers must be considered as well. The propagation delay from A14..19 and /AMS3 signal to /FPGA_CS output generation is a maximum of 10ns for the populated CPLD. The bus buffers have a maximum propagation delay of 4ns.

11.1 FPGA CONFIGURATION OPTIONS (J43)

When implemented in a target application the FPGA can be configured using the processors GPIO signals, or from an external EPCS serial configuration device. By default J43 is set for GPIO configuration of the FPGA. Refer to Table 21 below for a summary of the configuration options via J43.

Table 21: FPGA Configuration Options

DESCRIPTION	J43
Passive configuration mode via processor GPIO	1 + 2*
Active configuration mode via on-board EPCS device	2 + 3

* = Default

It should be noted that only one configuration option is available on the phyCORE-BF537 at a time. By default the passive mode is selected, and as such the EPCS serial configuration device is not populated on the module. If the active configuration mode is desired, be sure to indicate this to the PHYTEC sales representative.

During the firmware development stage the JTAG interface signals are made available at the phyCORE-connector for FPGA programming/configuration. Refer to Table 22 below for a signal list and phyCORE-connector pin locations.

Table 22: FPGA JTAG Signals at the phyCORE-connector X1

FPGA JTAG SIGNAL	phyCORE-CONNECTOR PIN LOCATION
FPGA_TDO	X1C75
FPGA_TMS	X1C73
FPGA_TCK	X1C76
FPGA_TDI	X1C74

11.1.1 PASSIVE FPGA CONFIGURATION

In passive configuration mode the FPGA is configured via 4 GPIO's from the processor. Processor signals PG15, PG14, PG13, and PG12 are used for this purpose. To enable sharing of these processor signals with the FPGA and with external functions the analog switch U30 is used. Control of the analog switch is accomplished with the external phyCORE-connector signal FPGA_PCTRL found on pin X1D30. By default this signal is pulled down on the phyCORE-BF537, routing the PG15..12 signals to the phyCORE-connector for external use as signals EXT_PG15..12. When

FPGA_PCTRL is driven to “1”, PG15..12 are routed to the FPGA passive programming pins, enabling configuration of the FPGA by the processor.

When the phyCORE-BF537 is used in conjunction with the phyCORE-BF537 Carrier Board, jumper JP21 provides a means to connect processor signal PG11 to the FPGA_PCTRL input. Example projects (Quartus II and VDSP++) are provided for configuring the FPGA via the ADSP-BF537 using PG11 as the FPGA_PCTRL source.

For information on configuring the FPGA in this mode, see the *Configuring Cyclone II Devices* chapter of the *Cyclone II Handbook, Volume 2*, available from Altera.

11.1.2 ACTIVE FPGA CONFIGURATION

In active configuration mode the FPGA reads configuration data from the EPCS external low-cost serial configuration device populated at U29. This serial configuration device can be programmed via the FPGA's JTAG port pins available at the phyCORE-connector during firmware development. See Table 22 above for a description of the JTAG pins dedicated to the FPGA and their locations on the phyCORE-connector.

For information on configuring the FPGA in this mode, see the *Configuring Cyclone II Devices* chapter of the *Cyclone II Handbook, Volume 2*, available from Altera.

11.2 FPGA BANK I/O VOLTAGE (J34, J35, J36)

Each FPGA bank provides separate power pins for configuring the I/O voltage level on the given bank. The phyCORE-BF537 provides the option to set the bank I/O voltage to either 3.3V, or the voltage provided by the external user supplied signal FPGA_VCCIO. By default jumpers J34, J35, and J36 are set to 1+2, providing a bank I/O voltage level of 3.3V Setting any of the three jumpers to the 2+3 connects the selected bank I/O voltage to the FPGA_VCCIO signal. The FPGA_VCCIO signal is a user supplied signal at phyCORE-connector pins X1D4 and X1D5. For permissible voltage ranges the Altera Cyclone II datasheet should be referenced for the particular FPGA in use. The phyCORE-BF537 can be populated with either the Cyclone II EP2C5 device, or the Cyclone II EP2C8 device.

It should be noted that only bank 1, bank 3, and bank 4 have configurable I/O voltage levels. Bank 2 of the FPGA is dedicated to the processor bus interface and has been permanently set to 3.3V. Refer to Table 23 below to configure the bank I/O voltage jumpers.

Table 23: FPGA Bank I/O Voltage Configuration

	DEFAULT SETTING		ALTERNATIVE SETTING	
J34	1 + 2	FPGA bank 1 I/O voltage set to 3.3V	2 + 3	FPGA bank 1 I/O voltage set to FPGA_VCCIO
J35	1 + 2	FPGA bank 4 I/O voltage set to 3.3V	2 + 3	FPGA bank 4 I/O voltage set to FPGA_VCCIO
J36	1 + 2	FPGA bank 3 I/O voltage set to 3.3V	2 + 3	FPGA bank 3 I/O voltage set to FPGA_VCCIO

12 DEBUG INTERFACE X2

The phyCORE-BF537 is equipped with a JTAG interface for downloading program code into internal controller RAM or for debugging programs currently executing. The JTAG interface extends out to 2.54 mm pitch pin header at X2 on the edge of the module, in addition to being made available at the phyCORE-connector X1. Figure 9 shows the position of the debug interface (JTAG connector X2) on the phyCORE-module. Even numbered pins are on the top of the module, starting with 2 on the right to 14 on the left, while odd number pins are on the bottom, starting from (as viewed from the top) 1 on the right to 13 on the left.

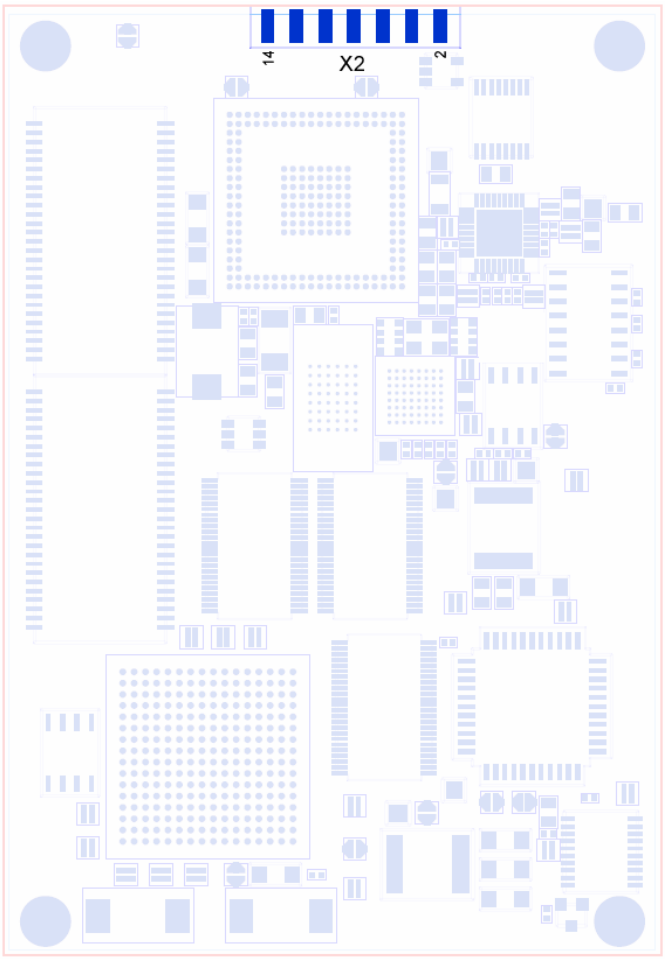

Figure 9: JTAG Interface X2 (Top View)

The JTAG edge card connector X2 provides an easy means of debugging the phyCORE-BF537 in your target system via an external emulator, such as one of the Analog Devices ICE emulators.

Alternatively when the phyCORE-BF537 is plugged onto its Carrier Board the DebugAgent debug interface becomes the primary debugging interface through the JTAG signals on the phyCORE-connector. The DebugAgent is a scaled down version of the high performance ICE emulators from Analog Devices and is suitable for initial test and development of software on the phyCORE-BF537.

Caution:
When the phyCORE-BF537 is used with the phyCORE-BF537 Carrier Board the edge card connector X2 can NOT be used by an external emulator. Use of an external emulator at X2 while the phyCORE-BF537 is plugged into its Carrier Board could result in damage to both the external emulator, and the DebugAgent circuitry on the Carrier Board. To make use of an external emulator when the phyCORE-BF537 is plugged into its Carrier Board, connector X10 on the Carrier Board should be used. Upon connection of an external emulator at X10, the DebugAgent goes into a pass-through mode, allowing safe connection of an external emulator.

Note:
The JTAG connector X2 only populates phyCORE-BF537 modules with order code PCM-033-xxxxxD. This version of the phyCORE module is included in all Rapid Development Kits (order code KPCM-033). JTAG connector X2 is not populated on phyCORE modules with order code PCM-033 that are intended for OEM implementation. However, all JTAG signals are also accessible at the phyCORE-connector X1 (Molex connectors). We recommend integration of a standard (2.54 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface. *See section 2 for details on the JTAG signal pin assignment.*

13 TECHNICAL SPECIFICATIONS

The physical dimensions of the phyCORE-BF537 are represented in Figure 10. The module's profile is approximately 9.1 mm thick, with a maximum component height of 4.5 mm on the bottom (connector) side of the PCB and approximately 2.9 mm on the top (microcontroller) side. The board itself is approximately 1.7 mm thick.

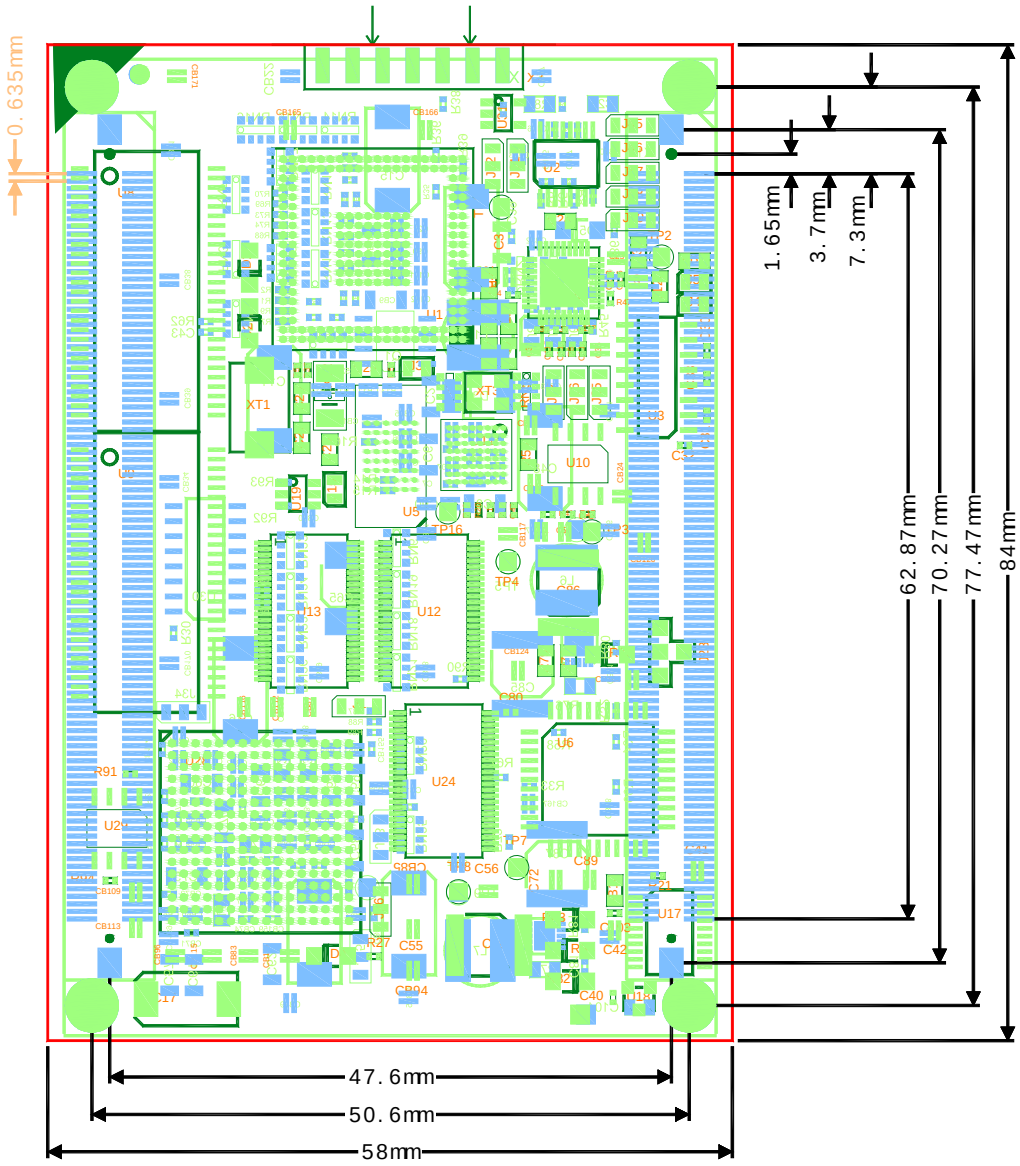

Figure 10: Physical Dimensions

Additional specifications:

• *Dimensions:*	*59 mm x 84 mm*
• *Weight:*	*Approximately 32 g for standard module configuration without FPGA*
• *Storage temperature:*	*-40°C to +90°C*
• *Operating temperature:*[1]	*-40°C to +85°C*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VCC 3.1V to TBD V* *VBAT 2.25V to 3.6V*
• *Power consumption:*	*Conditions:*
*VCC 3.3 V/**TBDmA** typical*	***VCC = 3.3 V, VBAT = 3.0V**,* *64MB SDRAM @ 125MHz, 4MB Flash,* *core @ 500MHz, most interfaces enabled*

These specifications describe the standard configuration of the phyCORE-LPCBF537 as of the printing of this manual.

1: Only valid for units without USB controller. Temperature range reduced to 0 - 70°C with USB controller installed.

14 HINTS FOR HANDLING THE phyCORE-BF537

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

15 THE phyCORE-BF537 ON THE phyCORE-BF537 CARRIER BOARD

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

15.1 CARRIER BOARD PERIPHERALS

The phyCORE-BF537 Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-BF537 Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

This modular development platform concept is depicted in Figure 11 and includes the following components and peripherals listed in *Table 24, Table 25, Table 26 and Table 27*. For a more detailed description of each peripheral refer to the appropriate section listed in the applicable table.

Table 24: Carrier Board Connectors

CONNECTORS		
REF DES	DESCRIPTION	SEE SECTION
X1	FPGA JTAG debugging interface	*15.3.3*
X2	Low-voltage power supply connectivity socket	*15.3.2*
X3	High speed user USB connector to interface phyCORE-BF537 on-board USB device controller	*15.3.5*
X4	Debug Agent USB connection to the PC for phyCORE-BF537 debugging	*15.3.6*
X5	5.0V voltage supply for external devices and subassemblies	*15.3.2.1*
X6	3.3V voltage supply for external devices and subassemblies	
X7	GND stud (for connection of GND signal of measuring devices such as an oscilloscope)	*N/A*
X10	External emulator connection interface	*15.3.6.1*
X12	Audio input jack	*15.3.7*
X13	Audio output jack	
X14	RJ45 Ethernet jack supporting the phyCORE-BF537 Ethernet interface	*15.3.8*
X15	phyCORE-connector for mating connectivity to the phyCORE-BF537 Single Board Computer	*15.3.1*
X16	GPIO expansion connector for easy access to phyCORE-BF537 signals	*15.3.9*

CONNECTORS		
REF DES	DESCRIPTION	SEE SECTION
X17	GND stud (for connection of GND signal of measuring devices such as an oscilloscope)	*N/A*
X18	CPLD JTAG programming interface	*15.3.4*
P1	Dual DB-9 female sockets for serial RS-232 interface connectivity	*15.3.10*
P2	Single DB-9 male socket for CAN interface	*15.3.11*
BAT1	Receptacle for an optional battery to support the ADSP-BF537 on-chip RTC	*15.3.12*

Table 25: Carrier Board Buttons

BUTTONS		
REF DES	DESCRIPTION	SEE SECTION
S1	System reset button	*15.3.15*
S2	User button #1	*15.3.13*
S3	User button #2	
S4	User button #3	
S5	User button #4	

Table 26: Carrier Board LEDs

LEDS		
REF DES	DESCRIPTION	SEE SECTION
D2	5V power LED indicator	*15.3.2*
D3	User LED #1 (red)	*15.3.14*
D4	User LED #2 (red)	
D5	User LED #3 (green)	
D6	User LED #4 (green)	
D8	Debug Agent “FLAG 1” indicator	*15.3.6*
D9	Debug Agent “FLAG 0” indicator	
D10	Debug Agent “MONITOR” indicator	
D11	Debug Agent “FPGA DONE” indicator	
D12	FPGA programming status indicator	*15.3.3*

Table 27: Carrier Board Potentiometers

POTENTIOMETERS		
REF DES	DESCRIPTION	SEE SECTION
R123	Optional A/D testing input	*15.3.18*

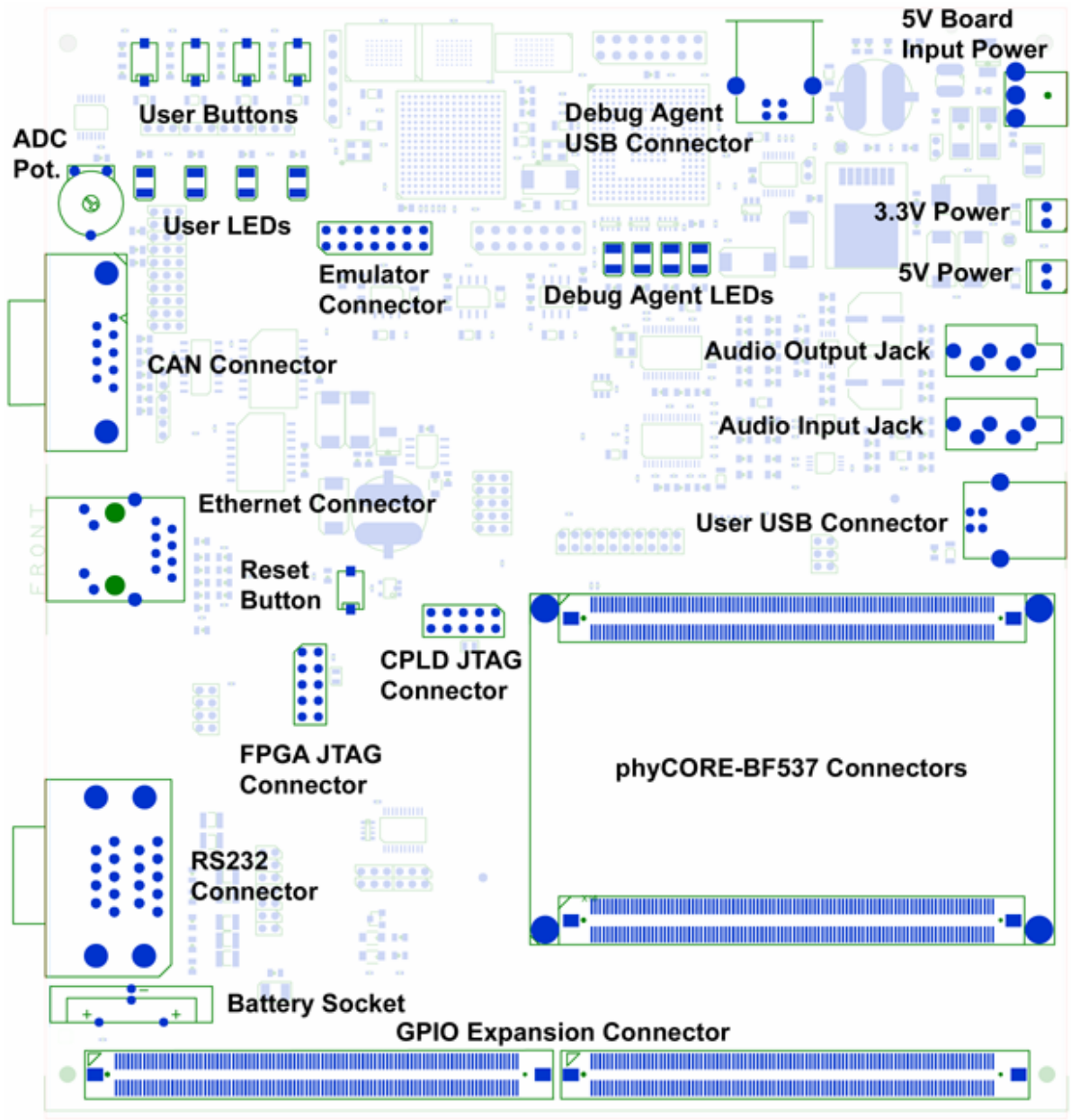

Figure 11: Component Locations on the phyCORE-BF536 Carrier Board

The GPIO expansion port connector X16 provides a 1:1 mapping of most of the phyCORE-BF537 connector X15 signals. Addditional signals generated on the Carrier Board are also routed to the GPIO expansion port connector X16. As an accessory a GPIO expansion board (part # PCM-977) is made available through PHYTEC to mate with the X16 connector on the phyCORE-BF537 Carrier Board. This expansion board provides a patch field for easy access to all signals, and additional board space for testing and prototyping. A summary of the signal mappings between X15, X16, and the patch field on the GPIO expansion board is provided in *section 15.4*.

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

15.2 JUMPERS

The phyCORE-BF537 Carrier Board comes preconfigured with 52 removable jumpers (JP). The jumpers allow the user flexibility of rerouting a limited amount of signals for development constraint purposes. Table 28 below lists the 52 removable jumpers, their default positions, and their functions in each position. Figure 12 depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

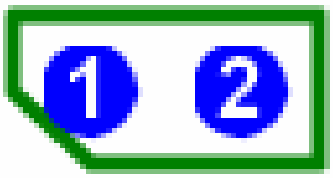

Figure 12: Typical Jumper Pad Numbering Scheme (removable jumpers)

The jumpers (J = solder jumper, JP = removable jumper) have the following functions:

Table 28: phyCORE-BF537 Carrier Board Jumper Settings

	DEFAULT SETTING		ALTERNATIVE SETTING		SEE SECTION
JP1	1+2	User button #1 (S2) output routed to processor signal PG0	2+3	User button #1 (S2) output routed to GPIO expansion connector as signal BTN1	*15.3.13*
JP2	1+2	User button #2 (S3) output routed to processor signal PG1	2+3	User button #2 (S3) output routed to GPIO expansion connector as signal BTN2	
JP3	1+2	User button #3 (S4) output routed to processor signal PG2	2+3	User button #3 (S4) output routed to GPIO expansion connector as signal BTN3	
JP4	1+2	User button #4 (S5) output routed to processor signal PG3	2+3	User button #4 (S5) output routed to GPIO expansion connector as signal BTN4	

	DEFAULT SETTING		ALTERNATIVE SETTING		SEE SECTION
JP5	2+3	Processor signal PF8 routed to LED1 (D3)	1+2	LED1 input source routed to GPIO expansion connector as signal LED1	*15.3.14*
JP6	2+3	Processor signal PF9 routed to LED2 (D4)	1+2	LED2 input source routed to GPIO expansion connector as signal LED1	
JP7	2+3	Processor signal PF14 routed to LED3 (D5)	1+2	LED3 input source routed to GPIO expansion connector as signal LED1	
JP8	2+3	Processor signal PF15 routed to LED4 (D6)	1+2	LED4 input source routed to GPIO expansion connector as signal LED1	
JP9[1]	closed	5V power supplied to Carrier Board	open	5V power removed from Carrier Board	*N/A*
JP10[2]	closed	3.3V power supplied to Carrier Board	open	3.3V power removed from Carrier Board	*N/A*
JP11	closed	Module watchdog disabled	open	Module watchdog enabled	*15.3.17*
JP12	open	RS-232 reset control disabled	closed	RS-232 reset control enabled	
JP13	open	Watchdog input signal WDI disconnected from processor signal PG9	closed	Watchdog input signal WDI connected to processor signal PG9	*15.3.17*
JP14	closed	UART0_TX_RS232 signal connected to DB-9 connector P1	open	UART0_TX_RS232 signal disconnected from DB-9 connector P1	*15.3.10*
JP15	closed	UART0_RX_RS232 signal connected to DB-9 connector P1	open	UART0_RX_RS232 signal disconnected from DB-9 connector P1	
JP16	closed	UART1_TX_RS232 signal connected to DB-9 connector P1	open	UART1_TX_RS232 signal disconnected from DB-9 connector P1	
JP17	closed	UART1_RX_RS232 signal connected to DB-9 connector P1	open	UART1_RX_RS232 signal disconnected from DB-9 connector P1	
JP18	closed	Audio interface clock loopback enabled	open	Audio interface clock loopback disabled	*15.3.7*
JP19	closed	Audio interface FS loopback enabled	open	Audio interface FS loopback disabled	

[1]: This jumper is intended as an access point to measure the total current on the carrier board + phyCORE-module from the 5V supply.

[2]: This jumper is intended as an access point to measure the total current on the carrier board + phyCORE-module from the 3.3V supply.

	Default Setting		Alternative Setting		See Section
JP20	closed	FPGA_VCCIO signal connected to 3.3V	open	FPGA_VCCIO signal disconnected from 3.3V	*15.3.3.1*
JP21	open	FPGA_PCTRL signal disconnected from processor signal PG11	closed	FPGA_PCTRL signal connected to processor signal PG11	
JP22	open	/FPGA_RST0 soft reset signal disconnected from processor signal PG10	closed	/FPGA_RST0 soft reset signal connected to processor signal PG10	
JP23	open	FPGA_B1_P3 signal disconnected from processor signal PG8	closed	FPGA_B1_P3 signal connected to processor signal PG8	
JP24	open	CAN power supplied through P2 disconnected from on-board 5V regulator	closed	CAN power supplied through P2 connected to on-board 5V regulator	*15.3.11*
JP25	1+2	R123 potentiometer output connected to module ADC signal ADC_IN0	2+3	R123 potentiometer output disconnected from module ADC signal ADC_IN0	*15.3.18*
JP26	2+3	Module ADC powered by Carrier Board 5.0V power supply	1+2	Module ADC power sourced from ADC_AVCC2 on the GPIO expansion connector	
JP27	2+3	CAN transceiver powered from on-board 5.0V power supply	1+2	CAN transceiver powered from VCAN+ supply through CAN connector P2	*15.3.11*
JP28	2+3	CAN isolator powered by on-board 3.3V supply	1+2	CAN isolator powered by regulated on-board 5.0V supply, or VCAN+ supply from CAN connector P2	
JP29	2+3	Processor signal PF14 connected to non-isolated CAN_EN signal	1+2 open	Processor signal PF14 connected to isolated CAN_EN signal Processor signal PF14 free for external use	
JP30	2+3	Processor signal PF15 connected to non-isolated /CAN_STB signal	1+2 open	Processor signal PF15 connected to isolated /CAN_STB signal Processor signal PF15 free for external use	
JP31	2+3	CAN transceiver GND isolated	1+2	CAN transceiver GND connected to Carrier Board GND plane	
JP32	2+3	CAN_EN signal isolation disabled	1+2	CAN_EN signal isolation enabled	

	Default Setting		Alternative Setting		See Section
JP33	2+3	/CAN_STB signal isolation disabled	1+2	/CAN_STB signal isolation enabled	15.3.11
JP34	2+3	/CAN_ERR signal isolation disabled	1+2	/CAN_ERR signal isolation enabled	
JP35	2+3	CAN_RXD signal isolation disabled	1+2	CAN_RXD signal isolation enabled	
JP36	2+3	CAN_TXD signal isolation disabled	1+2	CAN_TXD signal isolation enabled	
JP37	2+3	Processor signal SPI_SCK_PF13 connected to non-isolated /CAN_ERR signal	1+2 open	Processor signal SPI_SCK_PF13 connected to isolated /CAN_ERR signal Processor signal SPI_SCK_PF13 free for external use	
JP38	2+3	Processor signal CAN_RX connected to non-isolated CAN_RXD signal	1+2 open	Processor signal CAN_RX connected to isolated CAN_RXD signal Processor signal CAN_RX free for external use	
JP39	2+3	Processor signal CAN_TX connected to non-isolated CAN_TXD signal	1+2 open	Processor signal CAN_TX connected to isolated CAN_TXD signal Processor signal CAN_TX free for external use	
JP40	open	Processor signal BMODE2 disconnected from 3.3V	closed	Processor signal BMODE2 connected to 3.3V	15.3.16
JP41	open	Processor signal BMODE1 disconnected from 3.3V	closed	Processor signal BMODE1 connected to 3.3V	
JP42	open	Processor signal BMODE0 disconnected from 3.3V	closed	Processor signal BMODE0 connected to 3.3V	
JP43	closed	Processor signal PJ8 connected to audio ADC_DOUT signal	open	Processor signal PJ8 disconnected from audio ADC_DOUT signal	15.3.7
JP44	closed	Processor signal PJ6 connected to audio ADC_BCLK signal	open	Processor signal PJ6 disconnected from audio ADC_BCLK signal	
JP45	closed	Processor signal PJ7 connected to audio ADC_LRCLK signal	open	Processor signal PJ7 disconnected from audio ADC_LRCLK signal	

	Default Setting		Alternative Setting		See Section
JP46	closed	Processor signal PJ9 connected to audio DAC_BCLK signal	open	Processor signal PJ7 disconnected from audio DAC_BCLK signal	*15.3.7*
JP47	closed	Processor signal PJ10 connected to audio DAC_LRCLK signal	open	Processor signal PJ10 disconnected from audio DAC_LRCLK signal	
JP48	closed	Processor signal PJ11 connected to audio DAC_SDATA signal	open	Processor signal PJ11 disconnected from audio DAC_SDATA signal	
JP49	open	Processor signal SPI_MISO_PF12 disconnected from audio PF12_AUDIO_RESET signal	closed	Processor signal SPI_MISO_PF12 connected to audio PF12_AUDIO_RESET signal	*15.3.7*
JP50	closed	Audio ADC master mode enabled	open	Audio ADC master mode disabled	
JP51	open	CAN termination disabled	closed	CAN termination enabled	*15.3.11*
JP52	open	CAN termination disabled	closed	CAN termination enabled	

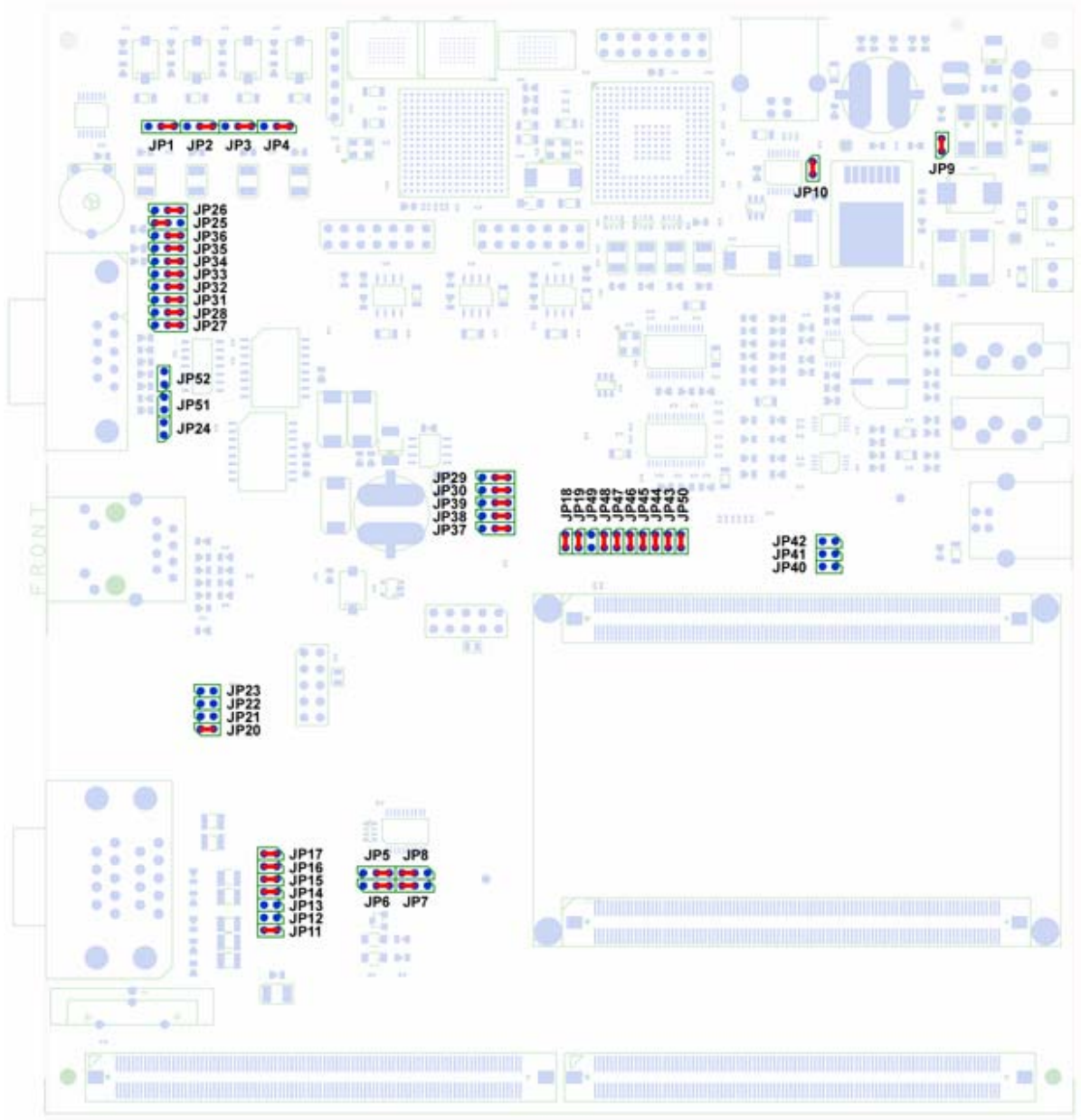

Figure 13: Jumper Locations and Default Settings

Figure 13 shows the location of the jumpers on the phyCORE-BF537 Carrier Board, along with their factory default settings. For a detailed description of jumper configuration, refer to section 15.3.

15.3 FUNCTIONAL COMPONENTS ON THE phyCORE-BF537 CARRIER BOARD

This section describes the functional components of the phyCORE-BF537 Carrier Board supported by the phyCORE-BF537 and appropriate jumper settings to activate these components. Depending on the specific phyCORE-BF537 module configuration, alternative jumper settings can be used. Each functional subsection shows a view of the Carrier Board with the connectors, components, and configuration jumpers emphasized for easy location. All jumpers have pin 1 located at the clipped corner of the jumper outline. Figure 12 in section 15.2 provides an illustration of the jumper numbering scheme.

15.3.1 phyCORE-BF537 CONNECTIVITY

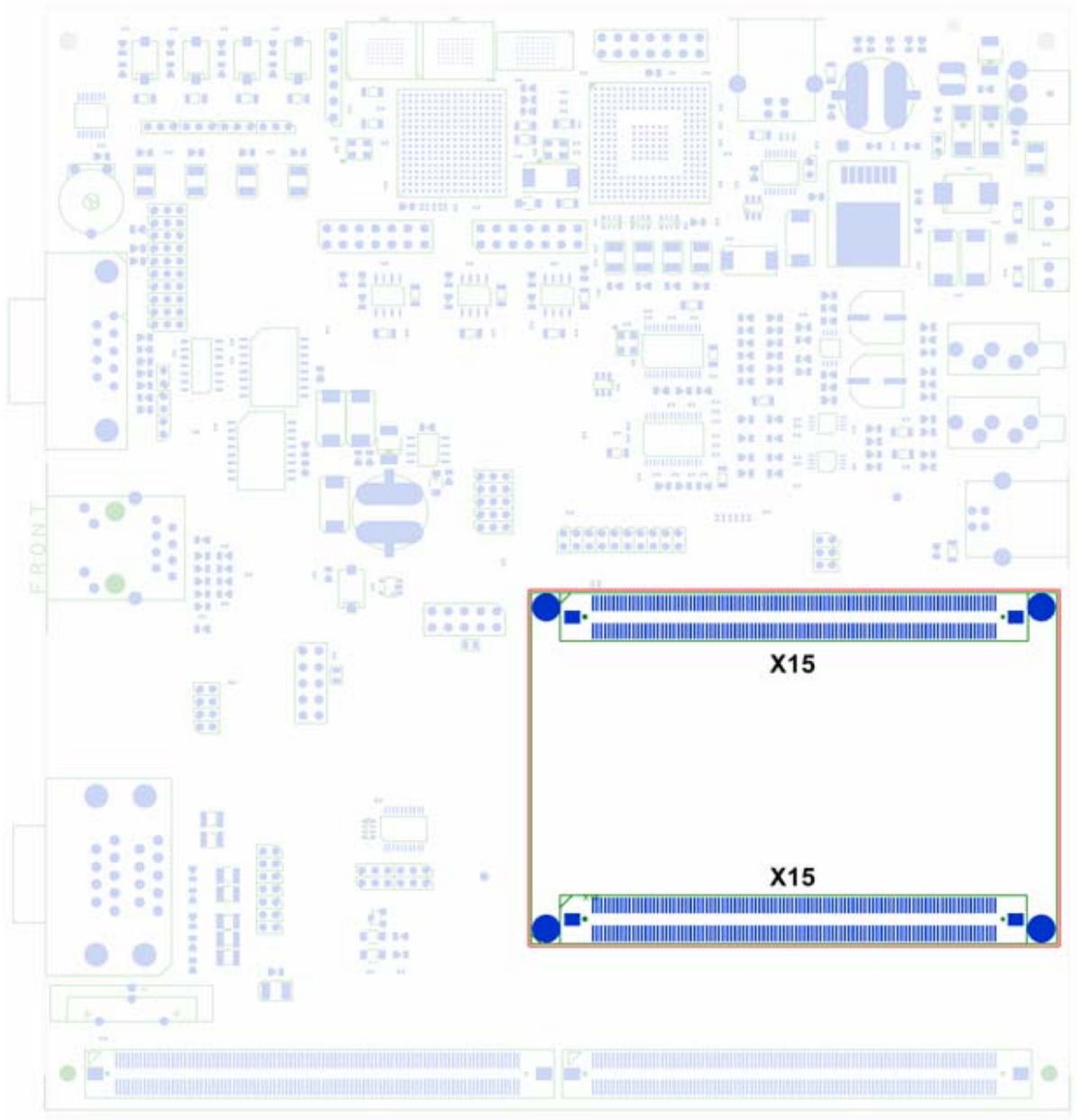

Figure 14: phyCORE-BF537 Mounting Connector

Connector X15 on the Carrier Board provides the phyCORE-BF537 connectivity. The connector is keyed for proper insertion of the module. Figure 14 above shows the location of connector X15.

15.3.2 POWER SUPPLY CONNECTIVITY

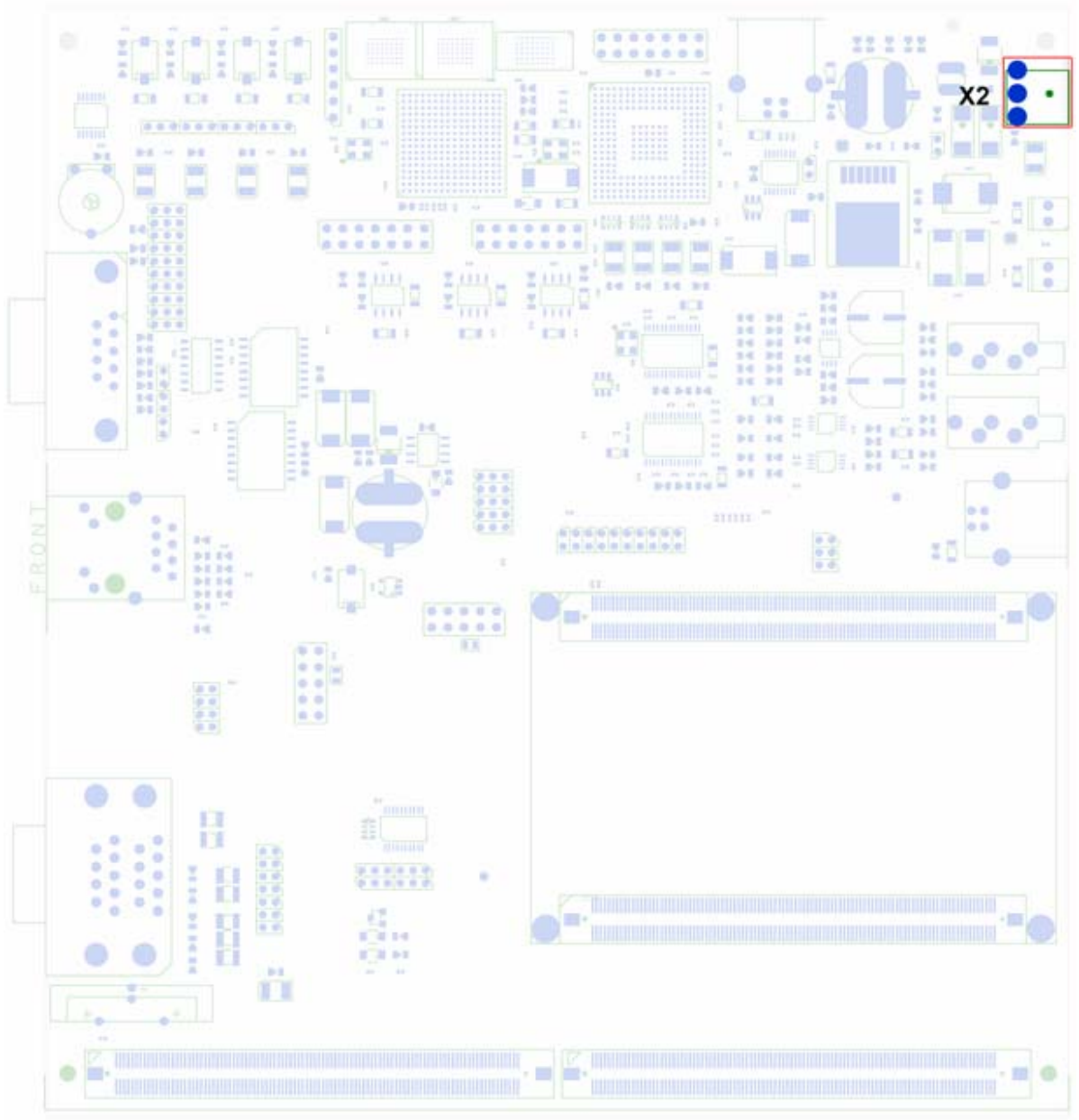

Figure 15: Carrier Board Power Supply Input

Caution:
Do not use a laboratory adapter to supply power to the Carrier Board! Power spikes during power-on could destroy the phyCORE module mounted on the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Permissible input voltage: +5 VDC regulated.

The primary input power to the phyCORE-BF537 Carrier Board is located at connector X2 as shown in Figure 15 above. The required load current capacity of the power supply depends on the specific configuration of the phyCORE-BF537 mounted on the Carrier Board, in addition to the particular interfaces enabled while executing software. An adapter with a minimum supply of 1500 mA is recommended.

To assist in current draw measurements from the 5V supplied to the board jumper JP9 can be used. By default jumper JP9 is closed, providing 5V power to the board (sourced from the 5V regulated supply at X2). JP9 can be removed as an easy access point to measure current if desired.

15.3.2.1 5.0V AND 3.3V POWER FOR EXTERNAL USE

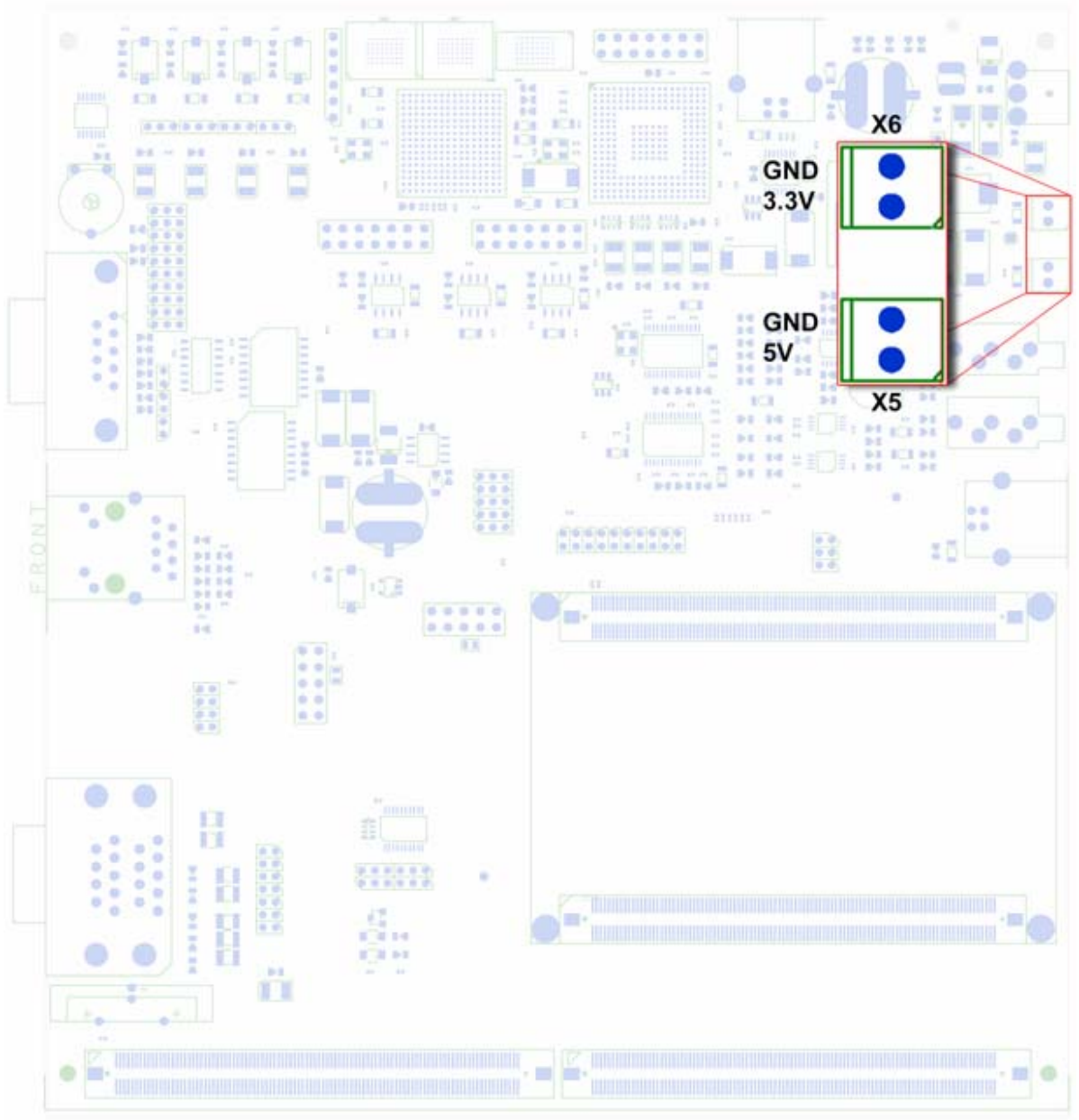

Figure 16: 5.0V and 3.3V Power Connectors

To facilitate power requirements when interfacing through the GPIO expansion port with custom circuitry connectors X5 and X6 are provided as shown in Figure 16 above. Connector X5 provides 5V for external use, while connector X6 provides 3.3V for external use. Current on both connectors should be limited to 100 mA for proper board operation.

15.3.3 FPGA Programming and Configuration

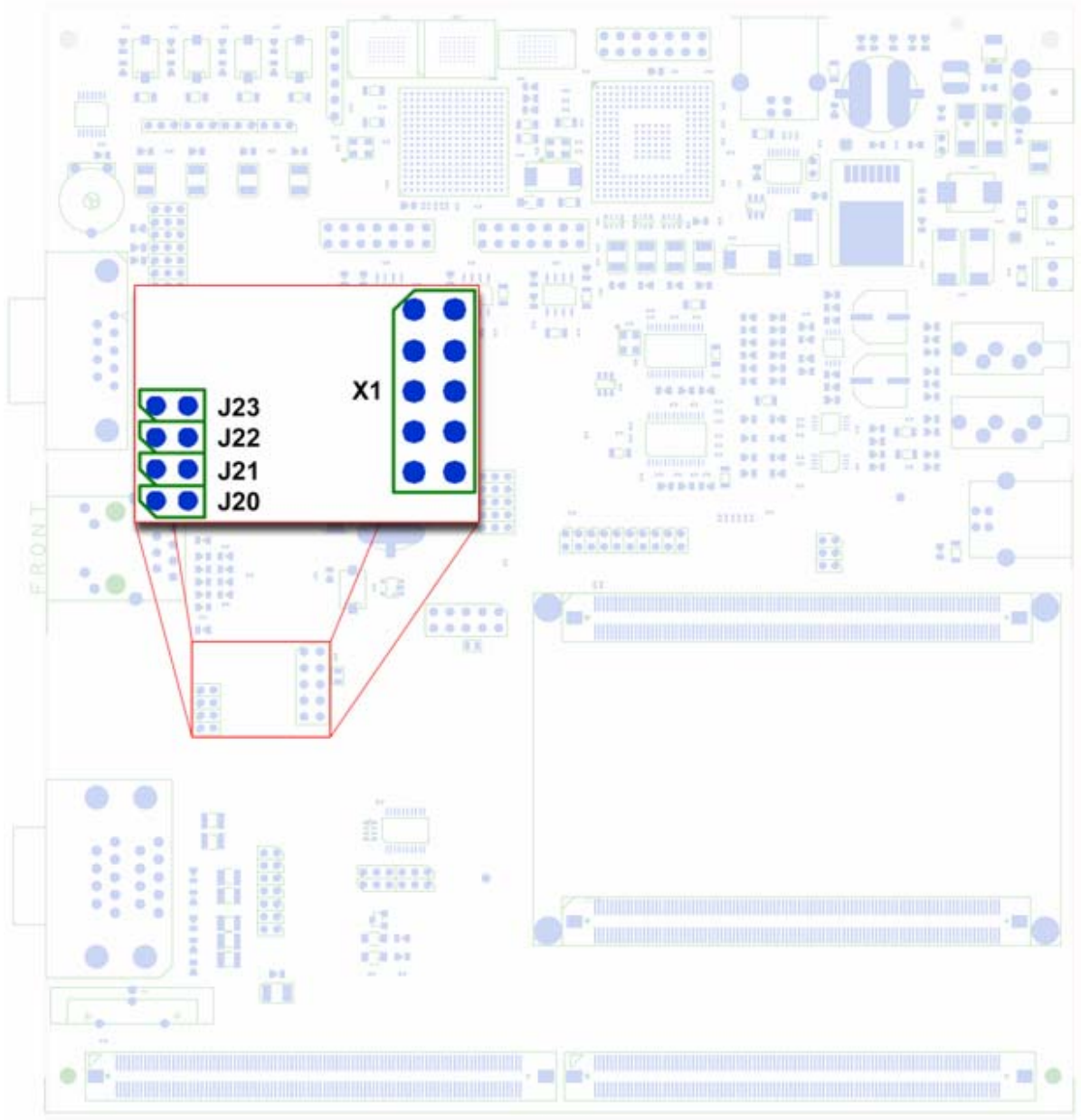

Figure 17: FPGA JTAG Connector and Configuration Jumpers

Connector X1 provides a means to connect an external JTAG download cable to the phyCORE-BF537 FPGA JTAG interface. In addition several configuration jumpers provide a means to connect essential FPGA functional signals to free processor GPIO.

Figure 17 above shows a detailed view of the JTAG connector X1, along with the location of pin 1 for proper connection of a download cable (such as the *USB-Blaster Download Cable* provided through Altera).

15.3.3.1 FPGA CONFIGURATION JUMPERS JP20-23

X1 FPGA JTAG programming connector. Pin 1 is marked by the clipped corner in Figure 17 above.

JP20 Connects the FPGA_VCCIO signal to the on-board 3.3V supply. By default this jumper is closed, providing 3.3V to FPGA_VCCIO. The default phyCORE-BF537 configuration does not use the FPGA_VCCIO signal to configure the FPGA bank voltages (see section 11.2 for details). If the phyCORE-BF537 is configured to use FPGA_VCCIO for particular FPGA banks then this jumper provides a convenient method for connecting FPGA_VCCIO to the 3.3V supply for testing purposes. Typically the need to use FPGA_VCCIO arises because a bank voltage other than 3.3V is required. In this case the desired voltage for the FPGA_VCCIO signal should be supplied through the GPIO expansion connector pins X16D4 and X16D5 (see Table 45 for patch field connectivity).

JP21 Connects processor signal PG11 to the FPGA_PCTRL signal. By default this jumper is open, disconnecting PG11 from FPGA_PCTRL. The FPGA_PCTRL signal is used in conjunction with passive configuration of the FPGA after module power-up. After power-up the FPGA_PCTRL signal should be driven HIGH to route the processor signals PG15..12 to the FPGA for configuration purposes. Once the FPGA has been configured the FPGA_PCTRL signal can be driven LOW to reroute the PG15..12 signals back to the phyCORE-connector for external use. See section 0 for a detailed explanation of FPGA_PCTRL.

JP22 Connects processor signal PG10 to the /FPGA_RST0 signal. By default this jumper is open, disconnecting PG10 from /FPGA_RST0. The /FPGA_RST0 signal is used as a software controllable reset source to the FPGA. This jumper should be closed to use PG10 as the reset source to the FPGA. Alternatively another processor signal could be connected to the /FPGA_RST0 signal via the GPIO expansion port.

JP23 Connects processor signal PG8 to the FPGA_B1_P3 signal. By default this jumper is open, disconnecting PG8 from the FPGA_B1_P3. The purpose of this jumper is to provide an interrupt source to the processor from the FPGA. Keep in mind that any suitable processor port pin capable of interrupts can be connected to any free FPGA I/O pin as an interrupt source. Jumper JP23 provides an easy means of using PG8 and FPGA_B1_P3 together.

15.3.4 CPLD Programming Interface

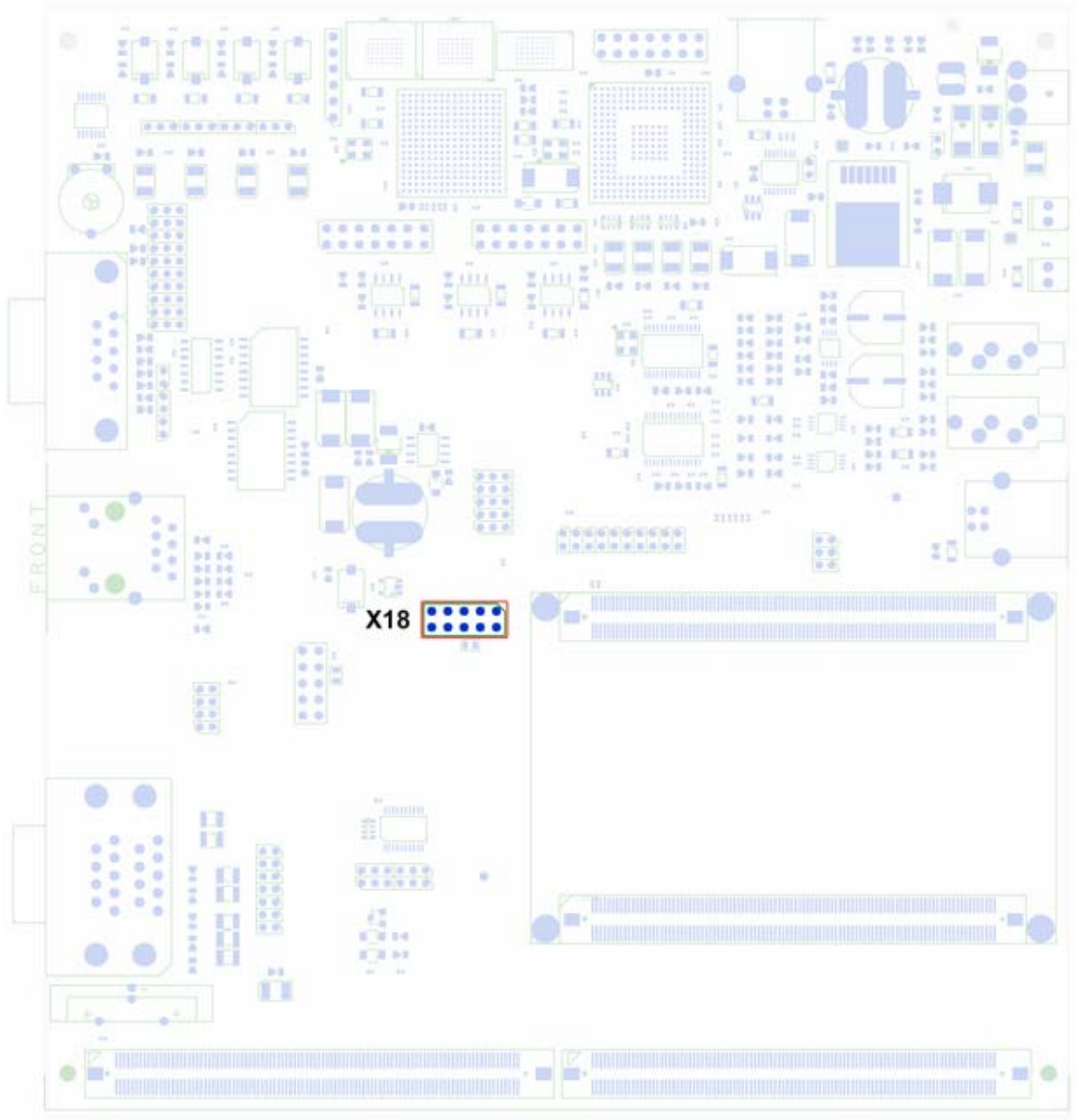

Figure 18: CPLD JTAG Connector

Connector X18 provides a means to connect an external JTAG download cable to the phyCORE-BF537 CPLD JTAG interface. Typically reprogramming of the CPLD will not be required due to factory preprogramming. However, JTAG access to the CPLD is provided for custom reconfiguration of the CPLD. Figure 18 above shows a detailed view of the CPLD JTAG connector, along with the location of pin 1 for proper connection of the download cable.

15.3.5 ACCESSING HIGH SPEED USB

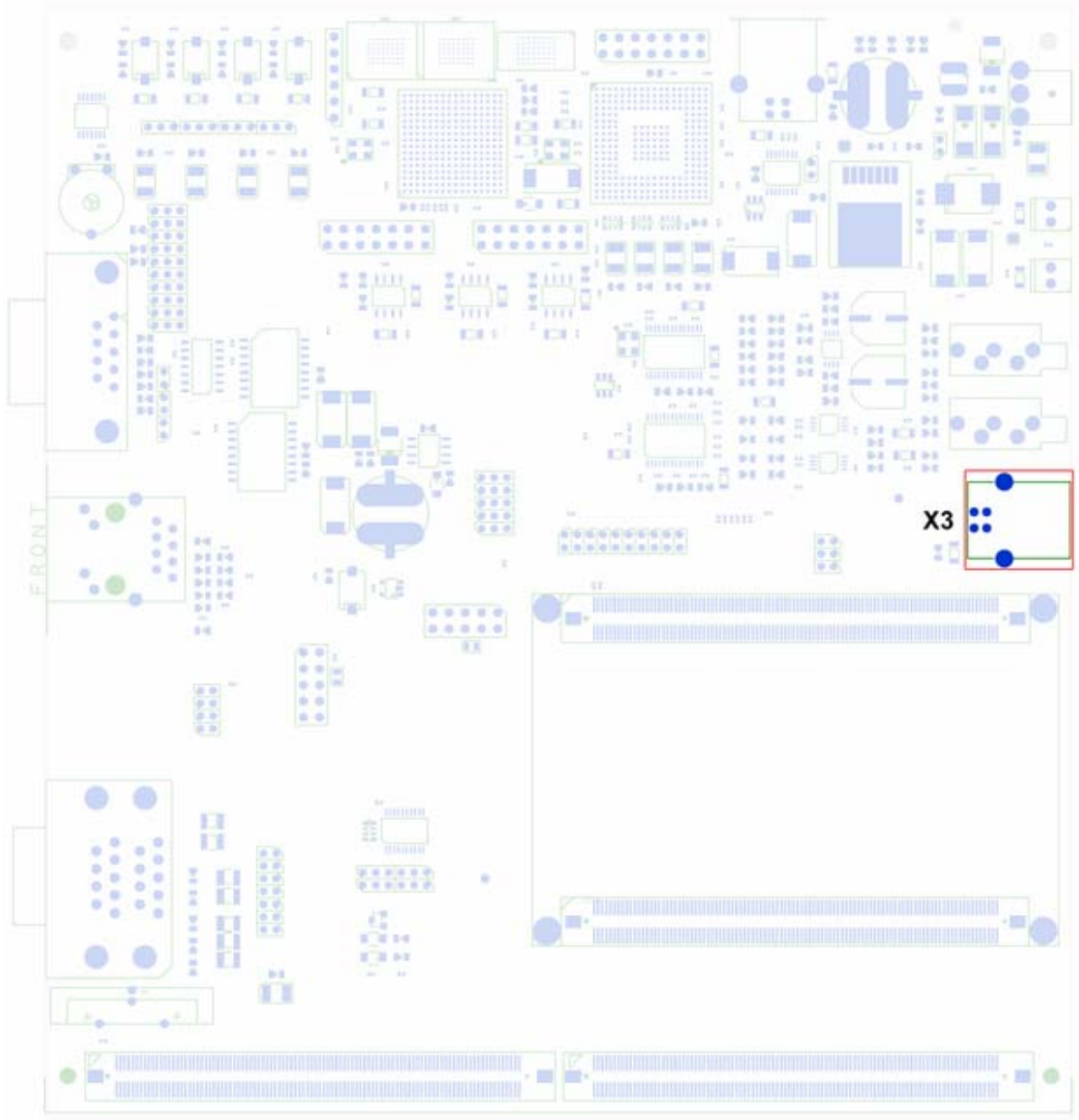

Figure 19: High Speed USB Device Connector

Connector X3 is provided to access the phyCORE-BF537 high speed USB device controller. Figure 19 above depicts the location of the USB connector for this purpose.

15.3.6 THE DEBUG AGENT DEBUGGING INTERFACE

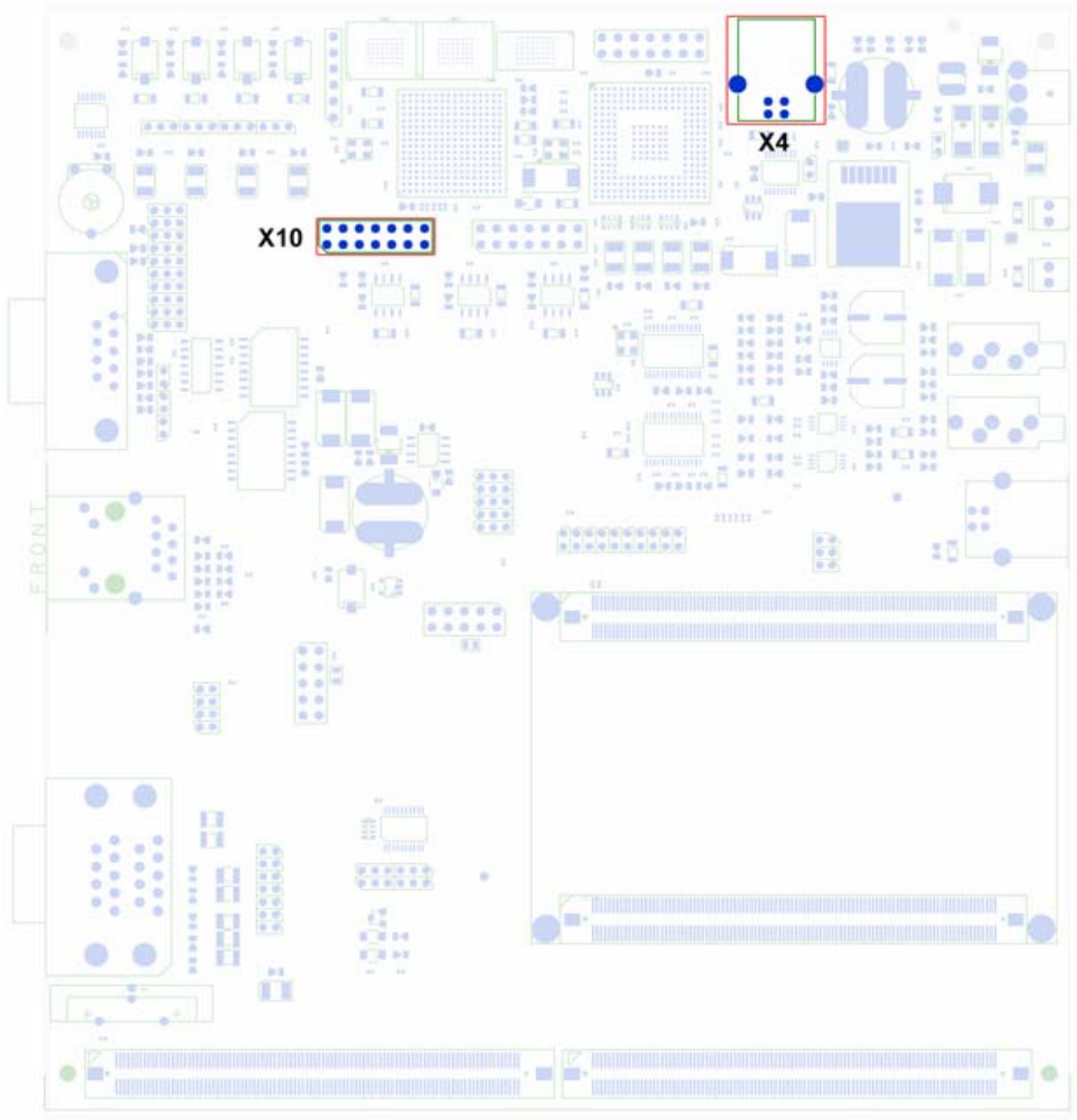

Figure 20: Debug Agent USB Connection Interface

To provide a convenient method for debugging software on the phyCORE-BF537 an integrated debugging interface known as the Debug Agent has been incorporated onto the Carrier Board. The Debug Agent allows speedy startup and programming of the phyCORE-BF537 without the need for a standalone emulator. To interface the Debug Agent a connection to a PC with the Visual DPS++ IDE installed using a standard A-to-B USB cable is required. For more information on using the DebugAgent please refer to the QuickStart document accompanying the Rapid Development Kit.

Figure 20 above shows the location of the Debug Agent USB connector X4.

15.3.6.1 CONNECTING AN EXTERNAL EMULATOR

If the use of an external emulator is desired then connector X10 in Figure 20 above can be used for this purpose. The Debug Agent will automatically detect the connection of an external emulator and activate pass-through mode, allowing the external emulator to take over.

15.3.7 THE AUDIO INTERFACE

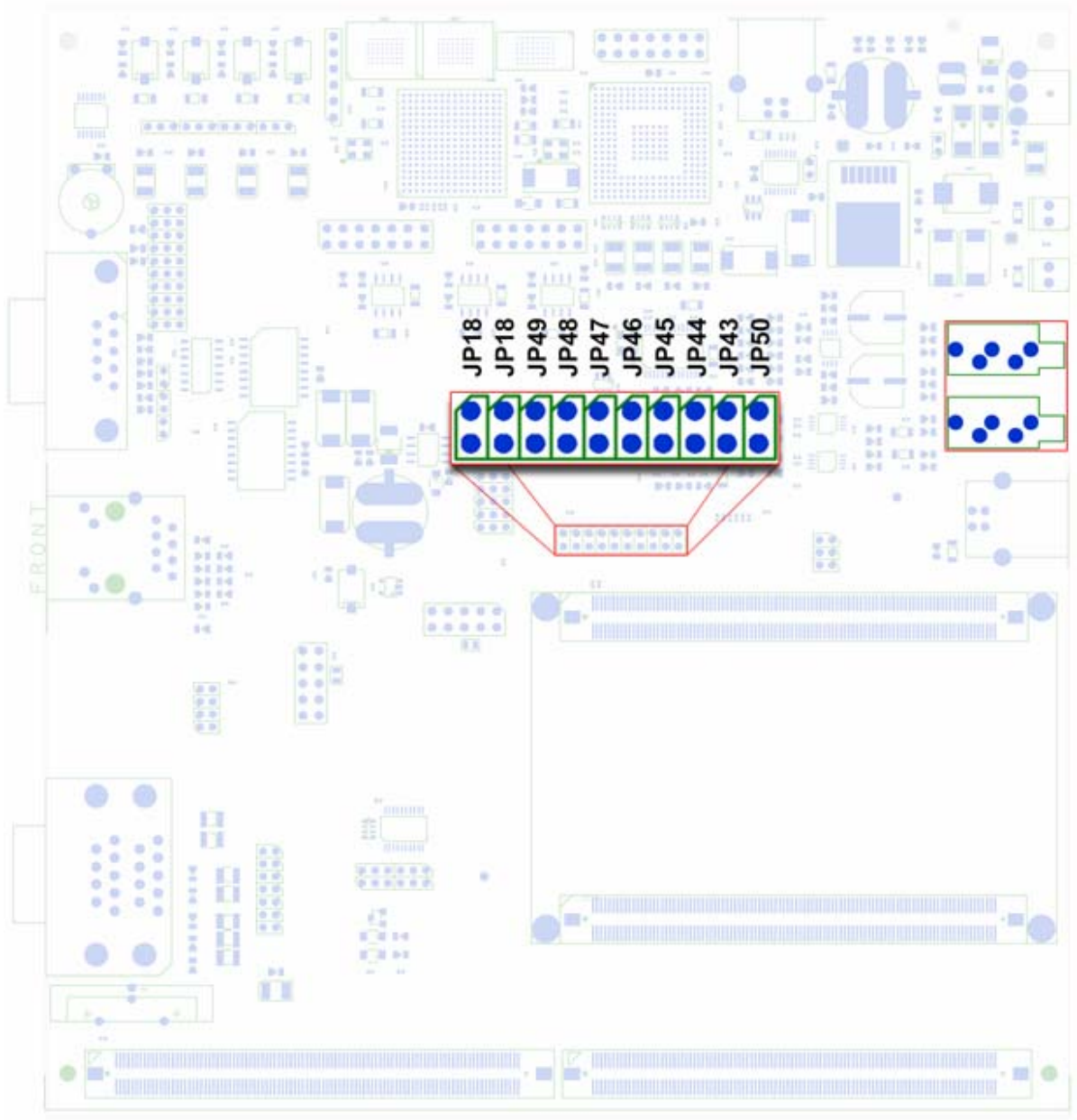

Figure 21: Audio Interface Connectors and Configuration Jumpers

The phyCORE-BF537 Carrier Board provides an audio interface to demonstrate the input and output of audio data via the SPORT interfaces on the phyCORE-BF537 SBC. The audio interface consists an ADC for digital conversion of analog audio input, providing one channel of stereo input, and a DAC for analog output of processed digital audio data, providing one channel of stereo output. A number of configuration jumpers allow for connectivity and configuration of the audio interface to the phyCORE-BF537. A detailed description of these configuration jumpers is described below.

X12	Stereo audio input jack – connect to external audio source, such as the line-out from your PC
X13	Stereo audio output jack – connect to external speakers, such as headphones
JP18	Clock loopback – Connects processor signal PJ6 (SPORT0 Receive Serial Clock) to processor signal PJ9 (SPORT0 Transmit Serial Clock). By default this jumper is closed, connecting PJ6 and PJ9. Remove this jumper if PJ6 or PJ9 are needed for external access and need not be connected together.
JP19	Frame Sync loopback – Connects processor signal PJ7 (SPORT0 Receive Frame Sync) to processor signal PJ10 (SPORT0 Transmit Frame Sync). By default this jumper is closed, connecting PJ7 to PJ10. Remove this jumper if PJ7 or PJ10 are needed for external access and need not be connected together.
JP43	Connects processor signal PJ8 (SPORT0 Receive Data Primary) to the audio ADC's data out signal ADC_DOUT. By default this jumper is closed, connecting PJ8 to ADC_DOUT. Remove this jumper if external access to PJ8 is required.
JP44	Connects processor signal PJ6 (SPORT0 Receive Serial Clock) to the audio ADC's serial bit clock signal ADC_BCLK. By default this jumper is closed, connecting PJ6 to ADC_BCLK. Remove this jumper if external access to PJ6 is required.
JP45	Connects processor signal PJ7 (SPORT0 Receive Frame Sync) to the audio ADC's left/right clock (word clock) signal ADC_LRCLK. By default this jumper is closed, connecting PJ7 to ADC_LRCLK. Remove this jumper if external access to PJ7 is required.
JP46	Connects processor signal PJ9 (SPORT0 Transmit Serial Clock) to the audio DAC's serial bit clock signal DAC_BCLK. By default this jumper is closed, connecting PJ9 to DAC_BCLK. Remove this jumper if external access to PJ9 is required.
JP47	Connects processor signal PJ10 (SPORT0 Transmit Frame Sync) to the audio DAC's left/right clock (word clock) signal DAC_LRCLK. By default this jumper is closed, connecting PJ10 to DAC_LRCLK. Remove this jumper if external access to PJ10 is required.
JP48	Connects processor signal PJ11 (SPORT0 Transmit Data Primary) to the audio DAC's serial data input signal DAC_SDATA. By default this jumper is closed, connecting PJ11 to DAC_SDATA. Remove this jumper if external access to PJ11 is required.
JP49	Connects processor signal PF12 to the audio reset circuit signal PF12_AUDIO_RESET. By default this jumper is open, disabling software controlled audio reset. If software controlled audio reset is desired (existing demos currently support this), then this jumper should be closed. It should be noted that the audio reset circuit is also connected to the system reset output signal /RESOUT from the phyCORE-module, and is reset on system power up.
JP50	ADC Master Mode select – By default this jumper is closed, setting the audio ADC into master mode, where the audio ADC generates the clock. When removed, the audio ADC is set into slave mode, where the processor generates the clock.

15.3.8 ETHERNET CONNECTIVITY

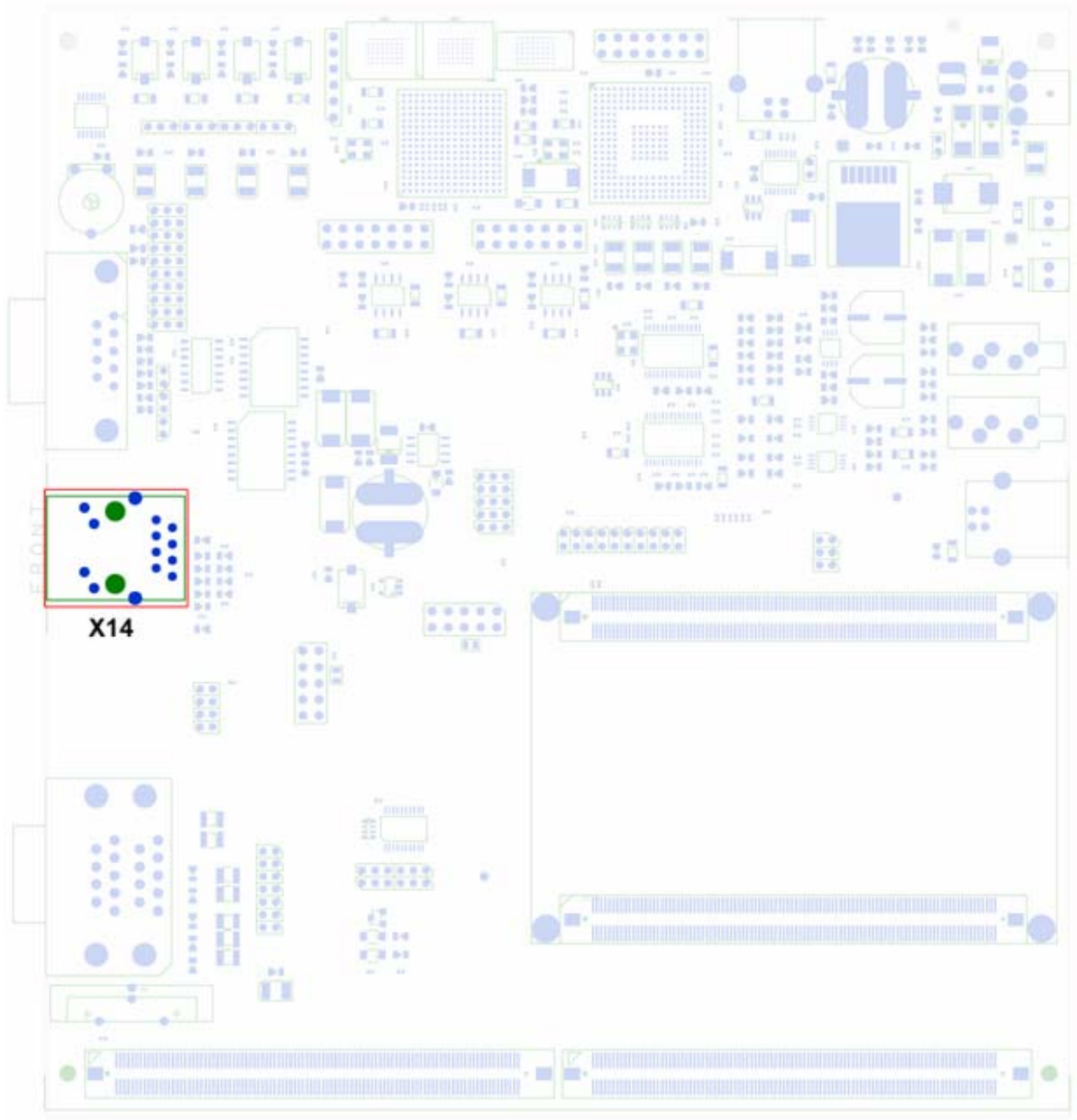

Figure 22: Ethernet Inteface Connector

Connector X14 provides a connection interface to the phyCORE-BF537 SBC Ethernet functionality. When connecting to the Ethernet it is permissible to use either a straight through cable, or a cross-over patch cable. The phyCORE-BF537 Ethernet PHY supports HP Auto-MDIX, removing the need for a particular cable type. HP Auto-MDIX automatically senses the RX/TX pins of the connecting device and configures the PHY RX/TX pins appropriately.

15.3.9 GPIO EXPANSION CONNECTOR

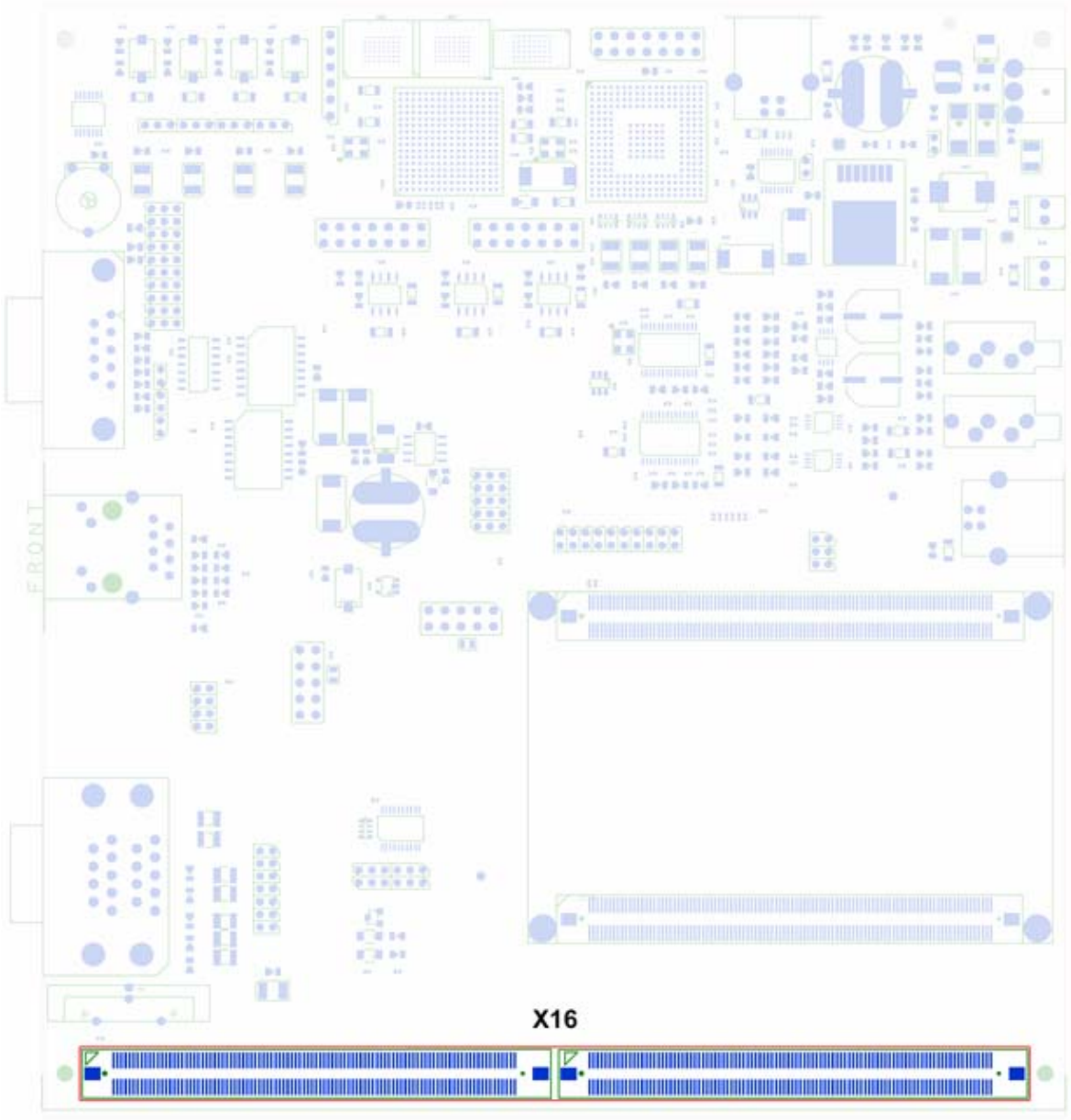

Figure 23: GPIO Expansion Interface Connector

Connector X16 provides a 1-to-1 mapping of a majority of the phyCORE-BF537 SBC connector signals. Select signals have been removed from the expansion connector for signal integrity reasons. The signals which have been removed are the User USB interface, JTAG, and Ethernet signals.

To connect to X16 PHYTEC provides a bare GPIO expansion interface PCB for prototyping purposes. The bare PCB contains a grid of solder holes, along with a patch field for easy connection to all X16 signals. Refer to section 15.4 for a detailed description of the patch field, along with a table show the location of all signals on the patch field.

15.3.10 RS-232 CONNECTIVITY

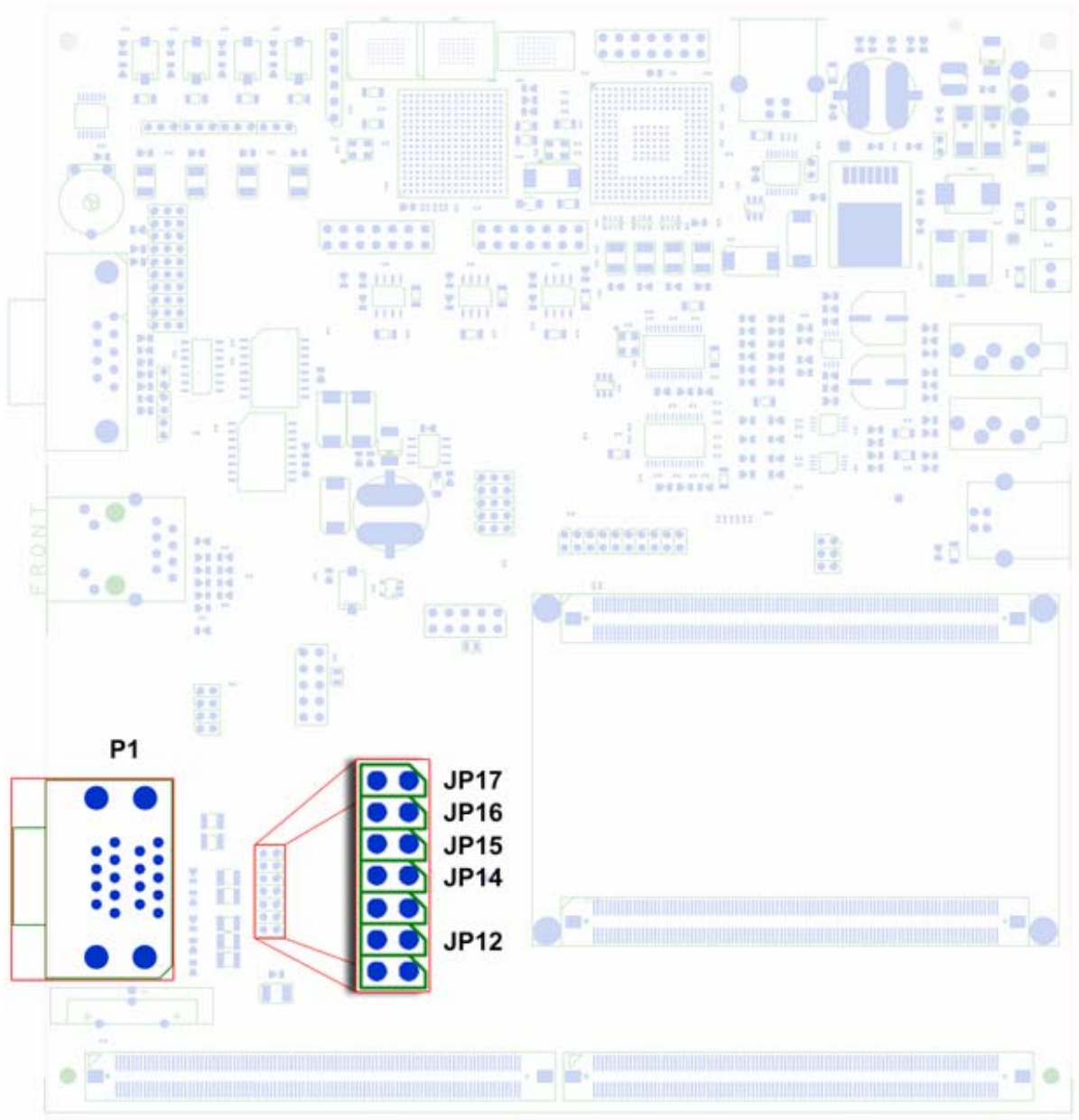

Figure 24: RS-232 Connector and Configuration Jumpers

Dual stacked DB9 connector P1 provides a connection interface to the phyCORE-BF537 SBC RS-232 signals from UART0 and UART1. Five configuration jumpers are provided to disconnect from P1 and to control system reset from UART0. A detailed description of the configuration jumpers is provided below.

JP12 Allows resetting of the module via the CTS signal from an external RS-232 interface connected to UART0 on P1A. By default this jumper is open, disabling module reset control via CTS. See Table X below for a description of the valid input ranges for the CTS signal.

JP14 Connects TX pin of P1A to UART0_TX_RS232 signal. By default this jumper is closed, connecting UART0_TX_RS232 to P1A.

JP15 Connects RX pin of P1A to UART0_RX_RS232 signal. By default this jumper is closed, connecting UART0_RX_RS232 to P1A.

JP16 Connects TX pin of P1B to UART1_TX_RS232 signal. By default this jumper is closed, connecting UART1_TX_RS232 to P1B.

JP17 Connects RX pin of P1B to UART1_RX_RS232 signal. By default this jumper is closed, connecting UART1_RX_RS232 to P1B.

Table 29: UART0 CTS Operating Limits

	MIN	MAX	UNITS
V_{IH}	2.5	15	V
V_{IL}	-15	1.0	V

15.3.11 CAN Configuration and Connectivity

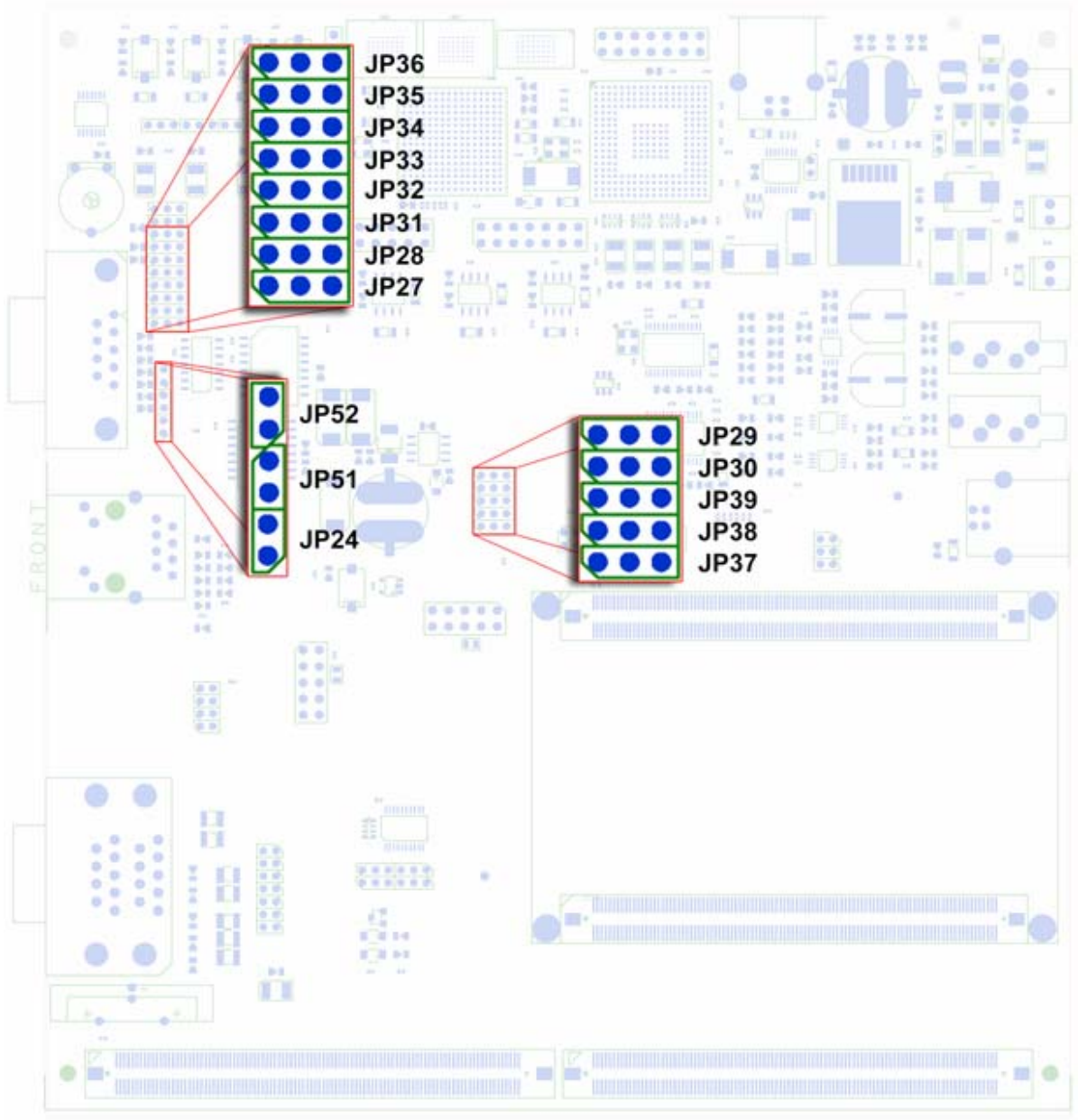

Figure 25: CAN Interface Connector and Configuration Jumpers

The phyCORE-BF537 Carrier Board is populated with a CAN transceiver and isolation couplers to support the phyCORE-BF537 SBC CAN interface. Connector P2 provides connectivity to the phyCORE-BF537 SBC CAN interface.

The CAN interface supports two modes of operation: 1) Isolated or (2) Isolation bypass (non-isolated). In mode (1) the CAN interface connection to the outside world is completely isolated from the CAN interface on the phyCORE-BF537 SBC. In mode(2) the isolation circuitry is bypassed, providing no protection from outside CAN interfaces to the Carrier Board and phyCORE-BF537 SBC. Mode (1) requires an external CAN voltage on the CAN connector P2 for proper operation. A switching regulator populated at U27 on the Carrier Board regulates the CAN input voltage down to 5V for on-board CAN transceiver and isolator operation. By default the Carrier Board is configured for mode (2) where isolation circuitry is bypassed. Table 30 below provides a description of the required jumper settings for both operation modes.

Table 30: CAN Operation Mode Jumper Settings

JUMPER	ISOLATION SETTING	ISOLATION BYPASS SETTING
JP24	closed	open
JP27	1 + 2	2 + 3
JP28		
JP29		
JP30		
JP31		
JP32		
JP33		
JP34		
JP35		
JP36		
JP37		
JP38		
JP39		

Caution:
The configuration jumpers listed in Table 30 above should not be set in any other manor than the two options listed, with one exception listed below. Configuring the jumpers differently could result in failed board operation and possible damage to the Carrier Board components and phyCORE-BF537 SBC.

If the CAN interface is not required then jumpers JP29, JP30, JP37, JP38, and JP39 provide the ability to disconnect the phyCORE-BF537 SBC signals from the CAN interface. It is permissible to completely remove these jumpers, leaving them open, and effectively disconnecting the signals from the CAN interface. A detailed description of the connected signals is provided below.

JP29 Open this to disconnect processor signal PF14 from the CAN interface.

JP30 Open this to disconnect processor signal PF15 from the CAN interface.

JP37 Open this to disconnect processor signal PF13 (SPI_SCK) from the CAN interface.

JP38 Open this to disconnect processor signal CAN_RX from the CAN interface.

JP39 Open this to disconnect processor signal CAN_TX from the CAN interface.

15.3.12 Optional External Battery

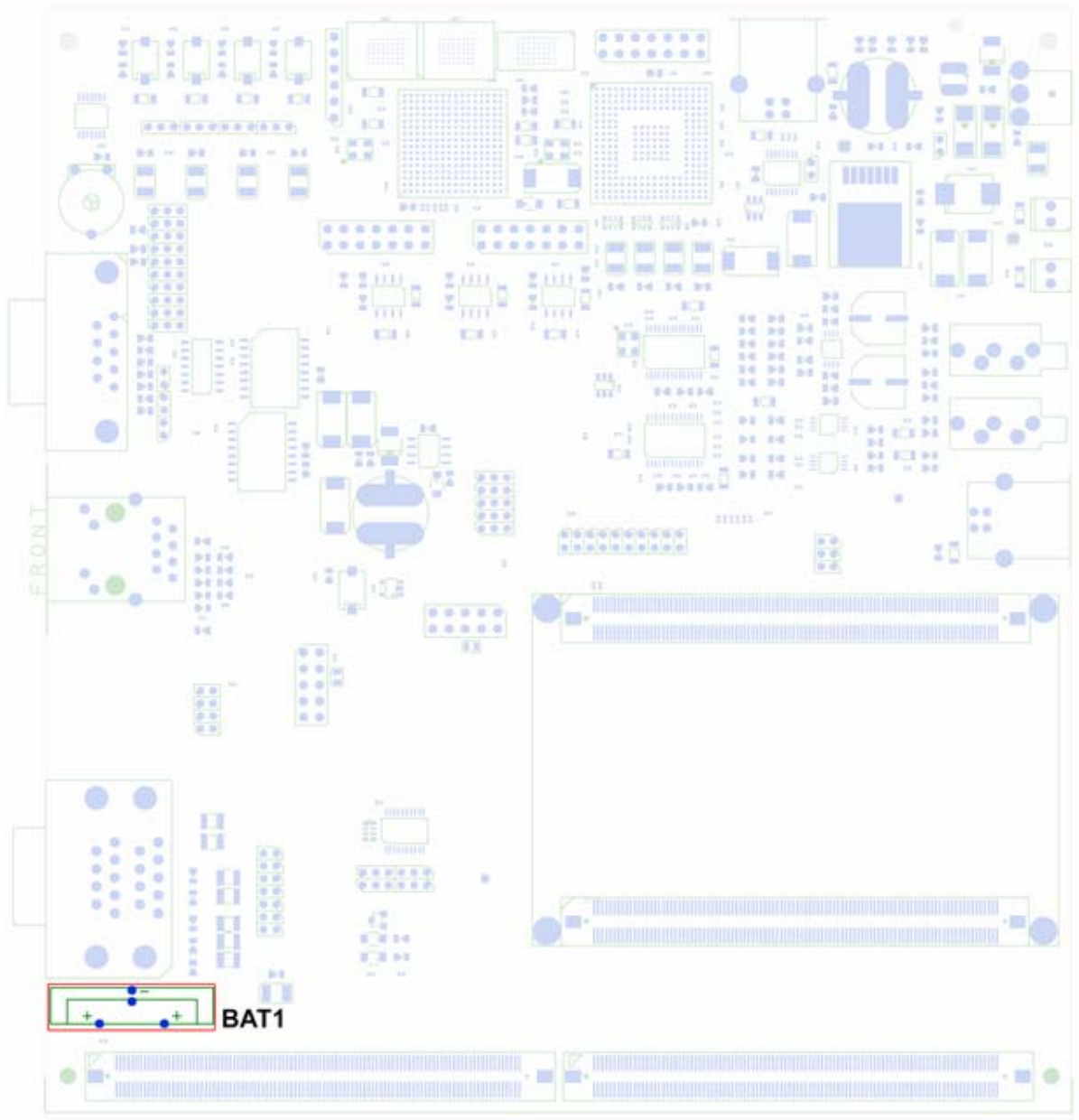

Figure 26: External Battery Connection Interface

Battery socket BAT1 is provided to mount an external 3.0V battery for operation with the phyCORE-BF537 SBC Real-Time Clock. By default this option is unpopulated on the Carrier Board. Without the battery installed the ADSP-BF537 processor on the phyCORE-BF537 SBC will be unable to maintain its Real-Time Clock contents in the absensce of power to the Carrier Board. If an external battery is required for this purpose it should be ordered directly from PHYTEC using part number BL-011. Alternatively an external 3.0V lithium-ion is recommended matching the polarity shown in Figure 26 above.

15.3.13 USER BUTTONS

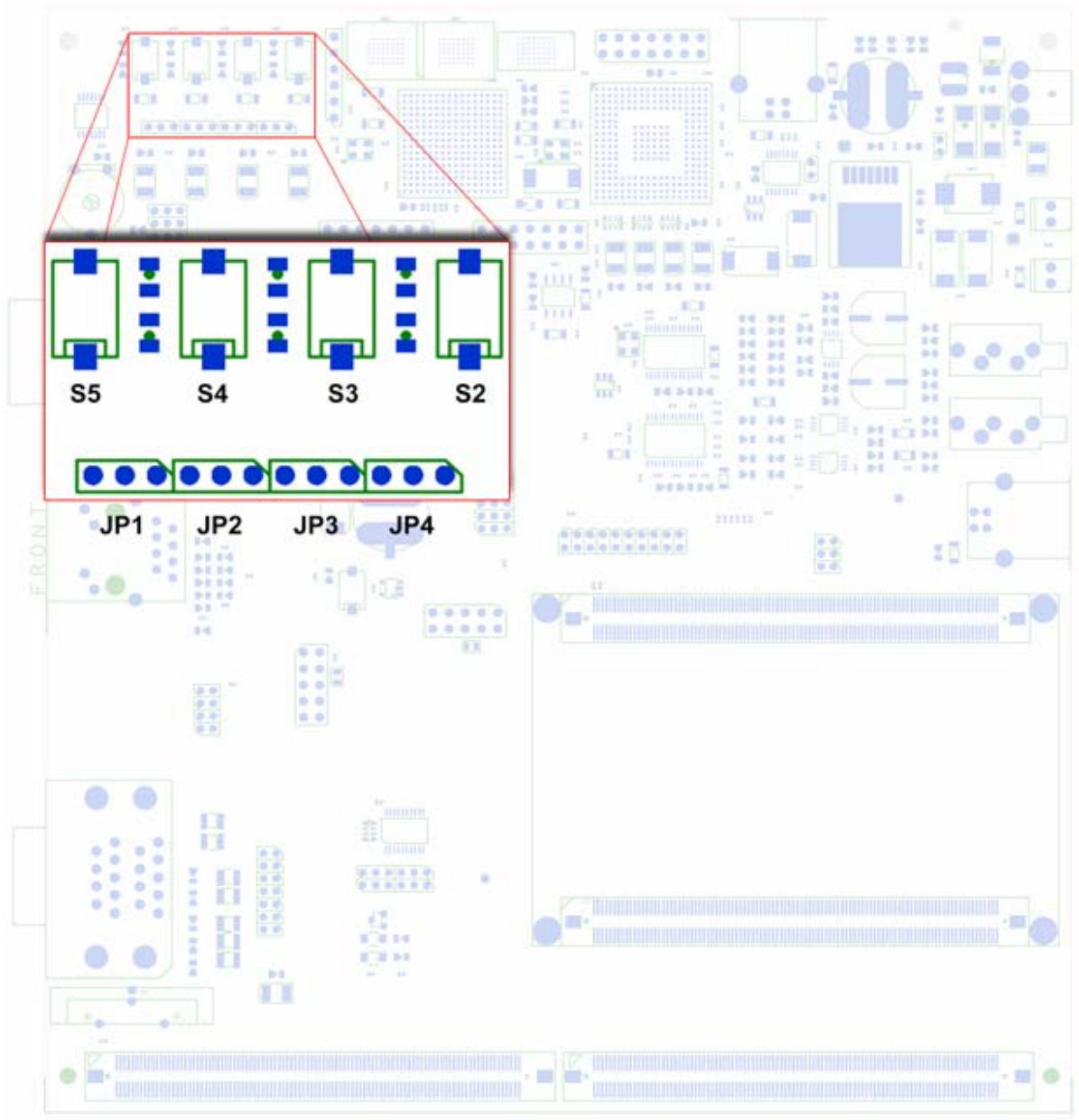

Figure 27: User Buttons

Four user configurable buttons S2, S3, S4, and S5 are provided on the Carrier Board for development purposes. Each button has an associated configuration jumper allow connection of the button output to a default phyCORE-BF537 SBC processor signal, or alternatively routing the button output to the GPIO expansion connector X16. When routed to the expansion connector it is then possible to connect the button output to all other processor signals available at the phyCORE-connector. The configuration jumpers also provide a method to disconnect default processor signals from buttons. Below a detailed description of button configuration and usage is presented.

S2 & JP1 Labeled “BTN1” on the Carrier Board. By default jumper JP1 connects the output of this button to processor signal PG0 when in the 1+2 position. Alternatively the 2+3 position routes the button output to the GPIO expansion connector X16 pin 87D as signal BTN1. Set this jumper to 2+3 or remove it completely to disconnect the button output from processor signal PG0.

S3 & JP2 Labeled “BTN2” on the Carrier Board. By default jumper JP2 connects the output of this button to processor signal PG1 when in the 1+2 position. Alternatively the 2+3 position routes the button output to the GPIO expansion connector X16 pin 88D as signal BTN2. Set this jumper to 2+3 or remove it completely to disconnect the button output from processor signal PG1.

S4 & JP3 Labeled “BTN3” on the Carrier Board. By default jumper JP3 connects the output of this button to processor signal PG2 when in the 1+2 position. Alternatively the 2+3 position routes the button output to the GPIO expansion connector X16 pin 90D as signal BTN3. Set this jumper to 2+3 or remove it completely to disconnect the button output from processor signal PG2.

S5 & JP4 Labeled “BTN4” on the Carrier Board. By default jumper JP4 connects the output of this button to processor signal PG3 when in the 1+2 position. Alternatively the 2+3 position routes the button output to the GPIO expansion connector X16 pin 91D as signal BTN4. Set this jumper to 2+3 or remove it completely to disconnect the button output from processor signal PG3.

15.3.14 USER LEDS

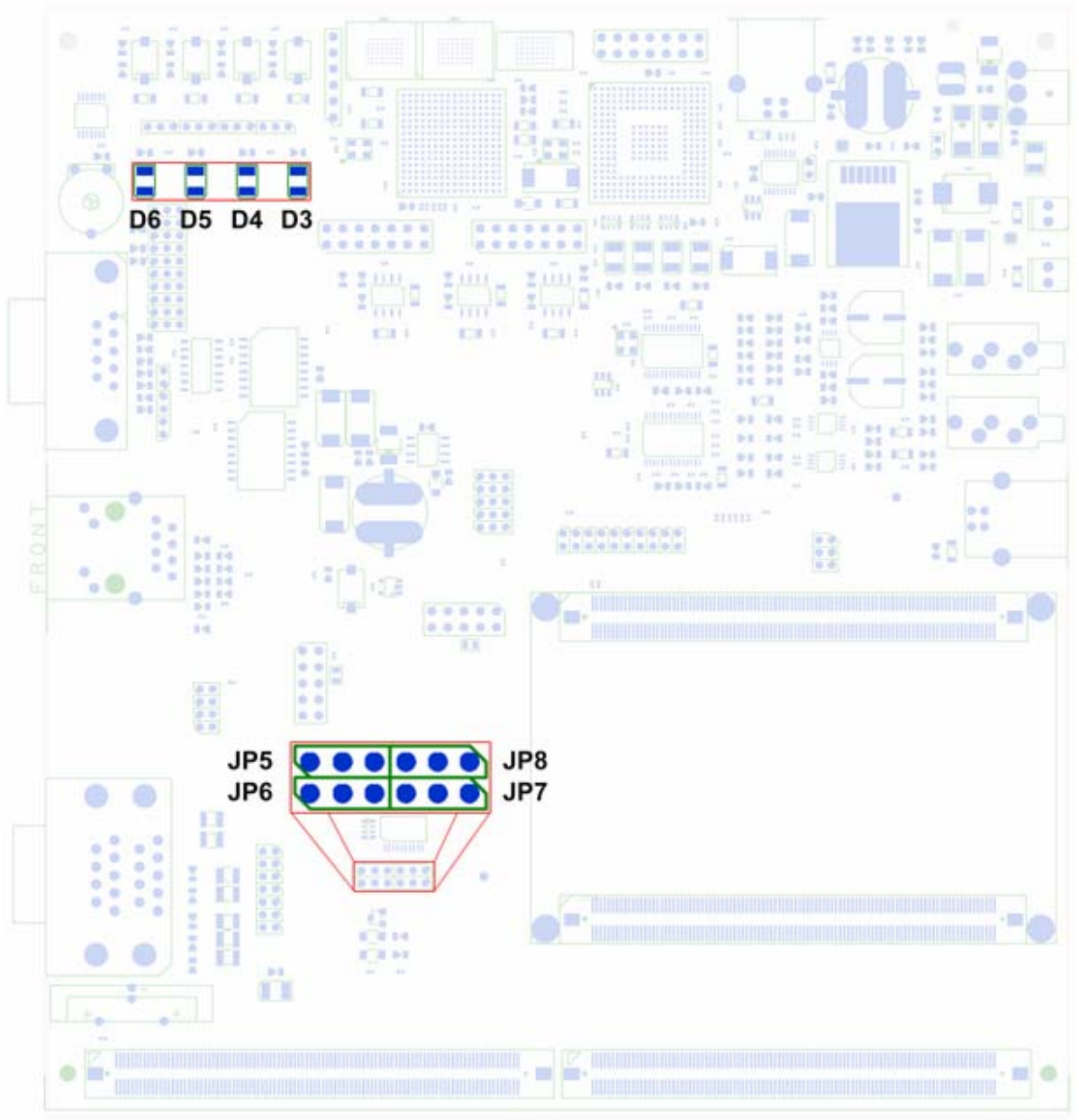

Figure 28: User LEDs

Four user controllable active high LEDs are provided on the Carrier Board for development purposes. Each LED is associated with a configuration jumper allowing configuration of the signal source driving the LED. All LED signals are buffered. A detailed explanation of the user LEDs and associated configuration jumpers is presented below.

D3 & JP5 Labeled “LED1” on the Carrier Board. By default jumper JP5 connects the input of this button to processor signal PF8 when in the 2+3 position. Alternatively the 1+2 position routes the LED input to the GPIO expansion connector X16 pin 88C as signal LED1. Set this jumper to 1+2 or remove it completely to disconnect the LED input from processor signal PF8.

D4 & JP6 Labeled “LED2” on the Carrier Board. By default jumper JP6 connects the input of this button to processor signal PF9 when in the 2+3 position. Alternatively the 1+2 position routes the LED input to the GPIO expansion connector X16 pin 89C as signal LED2. Set this jumper to 1+2 or remove it completely to disconnect the LED input from processor signal PF9.

D5 & JP7 Labeled “LED3” on the Carrier Board. By default jumper JP7 connects the input of this button to processor signal PF14 when in the 2+3 position. Alternatively the 1+2 position routes the LED input to the GPIO expansion connector X16 pin 90C as signal LED3. Set this jumper to 1+2 or remove it completely to disconnect the LED input from processor signal PF14.

D6 & JP8 Labeled “LED4” on the Carrier Board. By default jumper JP8 connects the input of this button to processor signal PF15 when in the 2+3 position. Alternatively the 1+2 position routes the LED input to the GPIO expansion connector X16 pin 91C as signal LED4. Set this jumper to 1+2 or remove it completely to disconnect the LED input from processor signal PF15.

15.3.15 SYSTEM RESET BUTTON

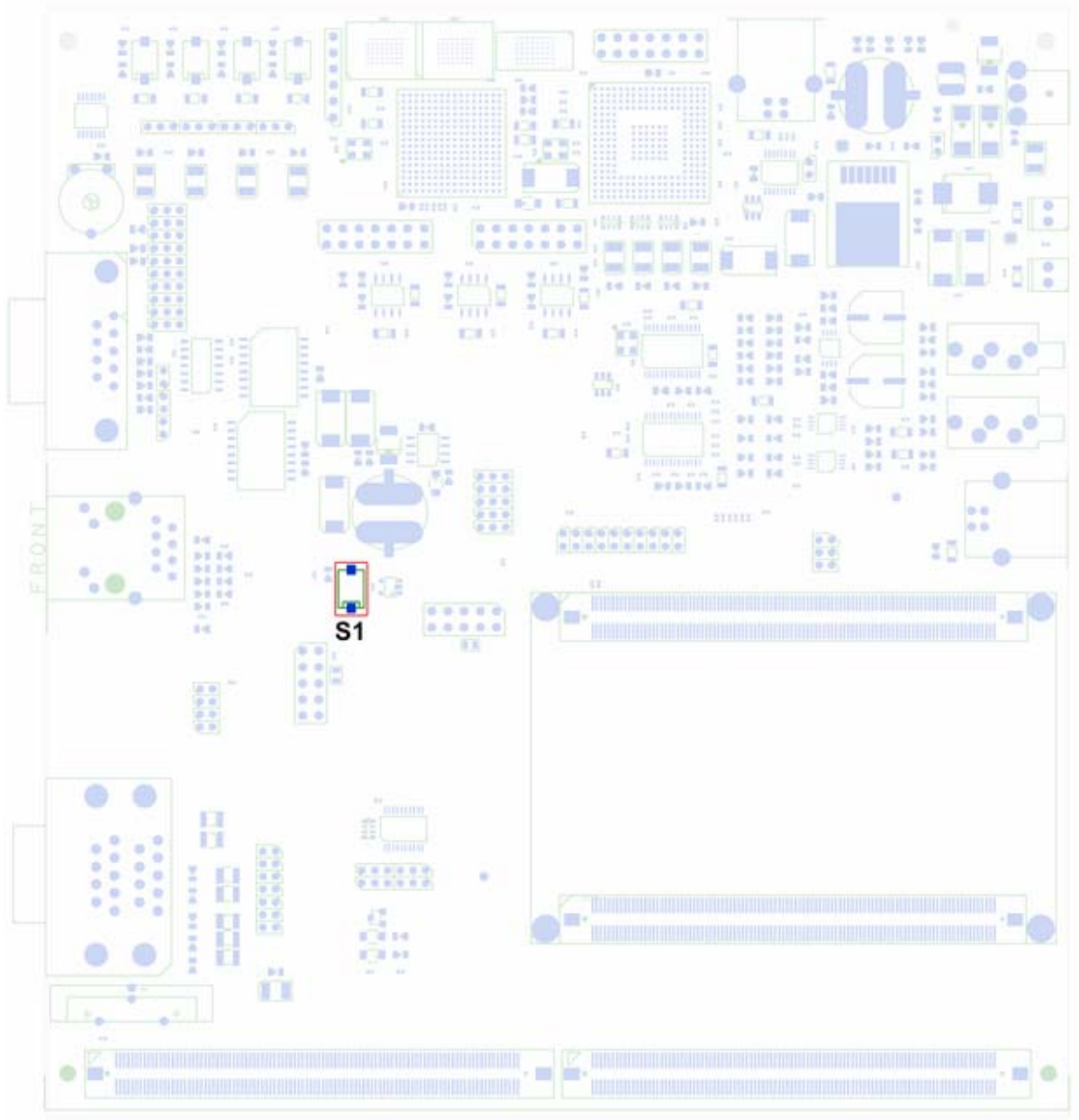

Figure 29: System Reset Button

The system reset button S1 is provided for manual external resets of the phyCORE-BF537. The reset button S1 provides momentary contact to GND on the /RESIN signal. Although S1 does not go through a debounce circuit the /RESIN signal to the phyCORE-BF537 is debouced by the on-board voltage supervisor, providing a timed processor reset duration of ~216ms (typical). To issue a system reset momentarily depress S1.

15.3.16 BOOT MODE SELECTION

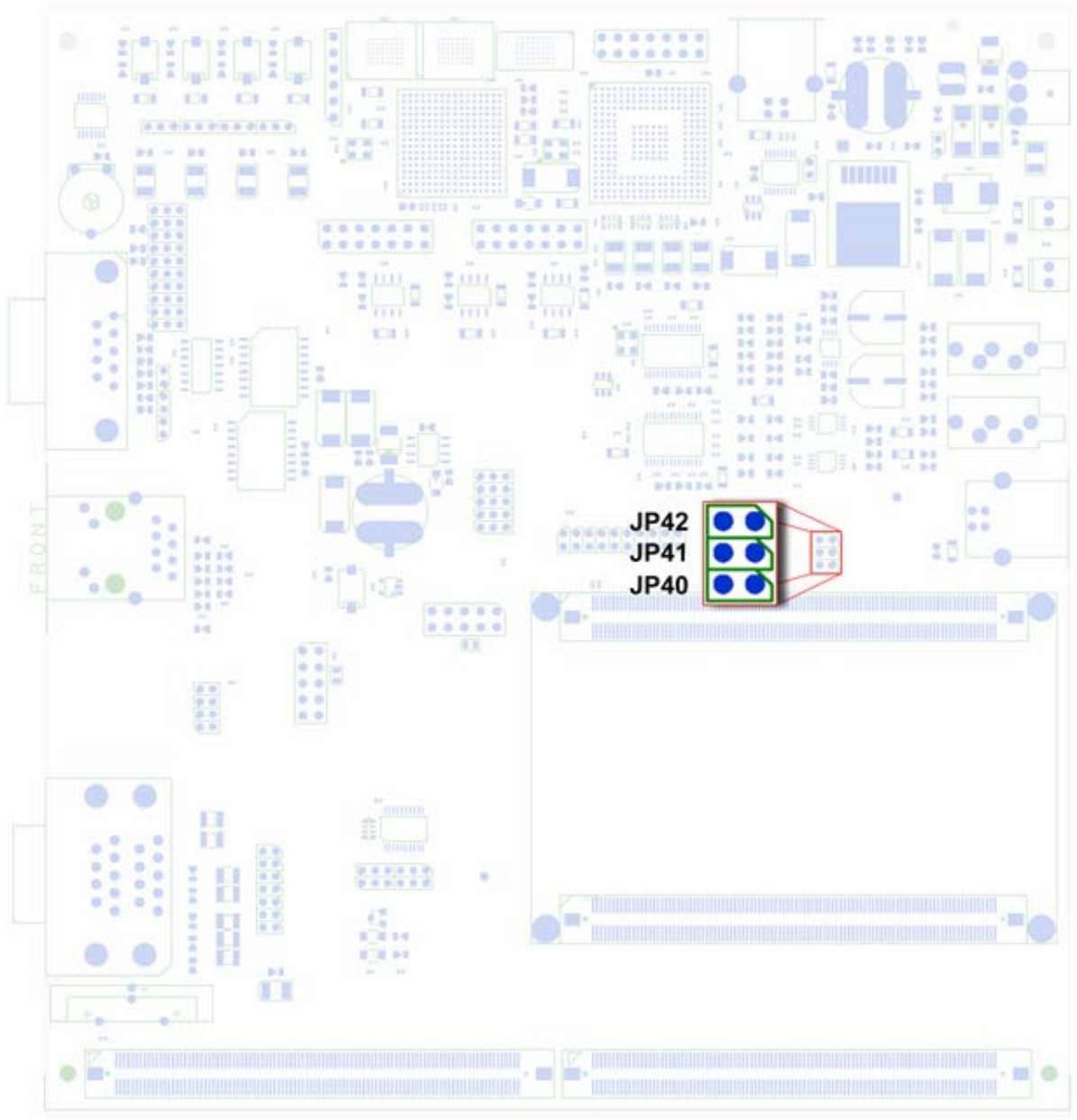

Figure 30: Boot Mode Selection Jumpers

The ADSP-BF537 supports 7 boot modes that are selectable via the external BMODE2..0 signals latched after a reset. By default the on-board pull-up and pull-down resistors select boot mode “001” as outlined in Table 31 below.

Table 31: Boot Mode Selection Settings using JP40, JP41, and JP42

BMODE2..0 CONFIGURATION	JP40	JP41	JP42	BOOT MODE
000	open	open	closed	Boot directly from external flash populated at U5 (bypass boot ROM)
001*	open	open	open	Boot from external flash at U5 using the on-chip boot ROM
010	open	closed	closed	Reserved
011	open	closed	open	Boot from external off-module SPI memory device
100	closed	open	closed	Boot from external SPI host
101	closed	open	open	Boot from internal on-module or external off-module TWI (I²C) memory device
110	closed	closed	closed	Boot from external TWI (I²C) host
111	closed	closed	open	Boot from external UART host

*= Default setting

15.3.17 USING THE WATCHDOG CIRCUIT

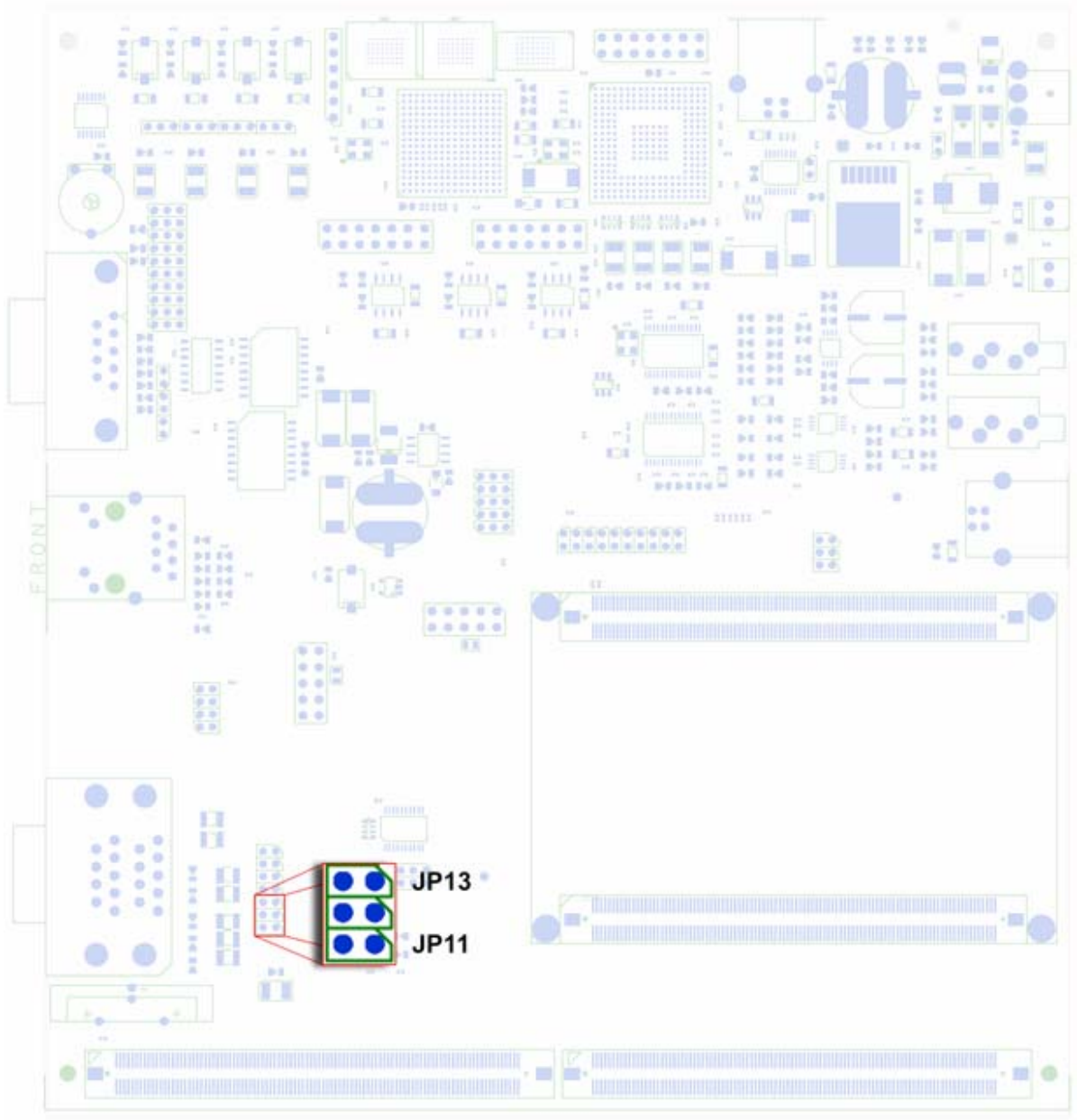

Figure 31: Watchdog Configuration Jumpers

Two configuration jumpers are provided on the Carrier Board to configure the watchdog functionality of the phyCORE-BF537 SBC. The watchdog circuit on the phyCORE-BF537 is responsible for resetting the processor in the event of a processor hang, or other unrecoverable error in which the normal execution flow is halted. Refer to section 4.2 for details on interfacing the phyCORE-BF537 watchdog circuit. A detailed explanation of the watchdog configuration jumpers is presented below.

JP11 Connects to the /WD_OFF signal of the phyCORE-BF537, controlling the enabling or disabling of the watchdog circuit. By default this jumper is installed and the watchdog circuit on the phyCORE-BF537 is disabled. To enable the watchdog, remove this jumper.

JP13 Connects processor signal PG9 to watchdog input signal WDI on the phyCORE-BF537. By default this jumper is open, disconnecting PG9 from WDI. To use PG9 as the watchdog input source, close this jumper.

15.3.18 ADC INTERFACE AND CONFIGURATION

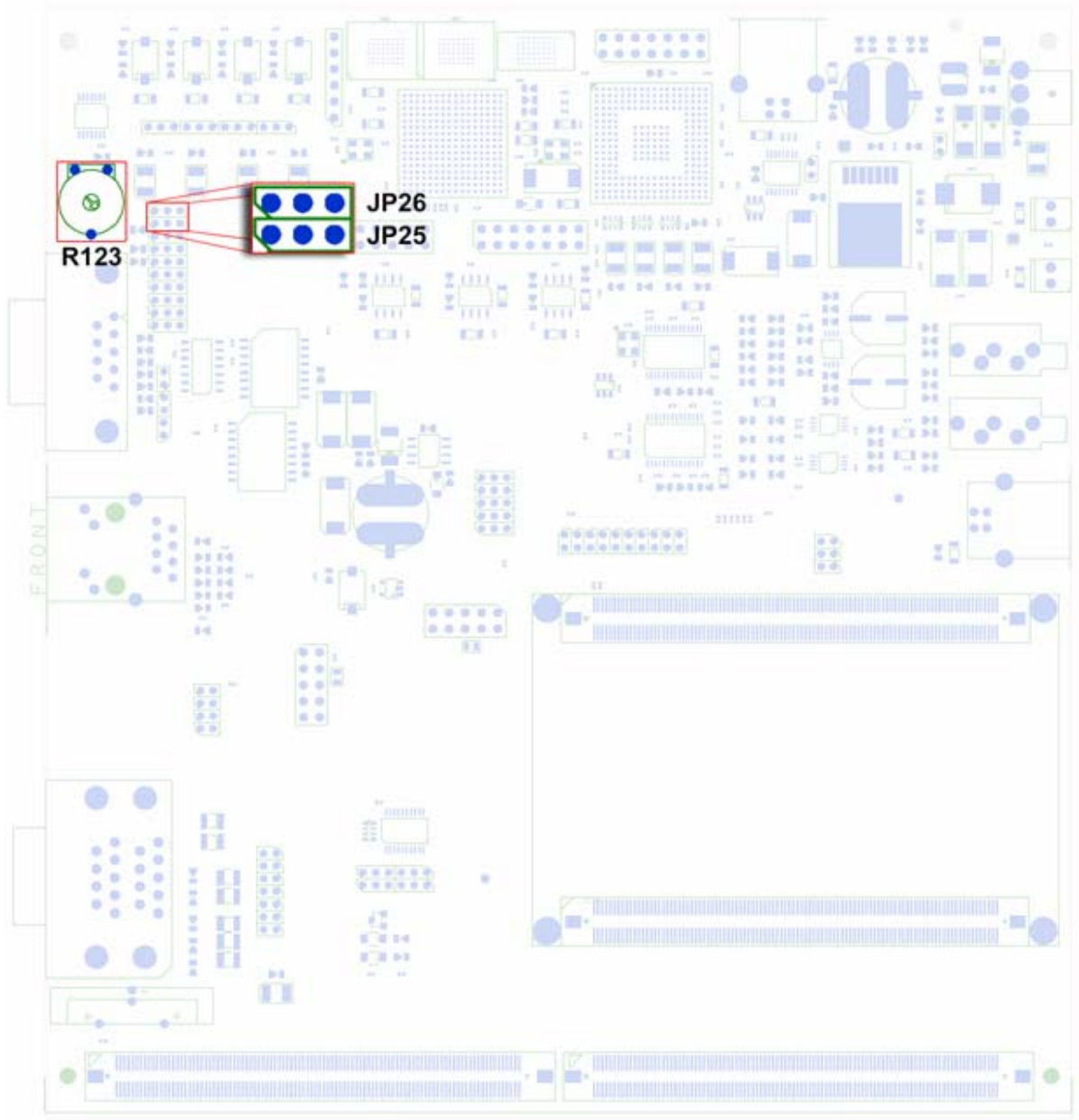

Figure 32: ADC Configuration Jumpers

Two configuration jumpers and a potentiometer populate the Carrier Board to facilitate interfacing the phyCORE-BF537 on-board ADC. Jumper JP26 provides ADC power control, and JP25 provides potentiometer output routing control. A detailed description of the jumper configuration is provided below.

JP25 Connects ADC channel 0 signal ADC_IN0 from the phyCORE-BF537 SBC to the potentiometer output when in the default position of 1+2. Alternatively this jumper can be set to 2+3 and instead route the potentiometer output to the GPIO expansion connector X16 pin 95D. Set this jumper to 2+3 or remove it completely to disconnect the ADC_IN0 signal from the potentiometer.

JP26 Connects the ADC power supply input pins on the phyCORE-BF537 SBC to the on-board 5V power supply when in the default position of 2+3. Alternatively this jumper can be set to the 1+2 position, routing the ADC_AVCC2 signal from the GPIO expansion connector X16 pin 95C to the ADC power supply pins on the phyCORE-BF537. Set this jumper to 1+2 when the need for a different supply voltage other than 5V to the ADC is desired.

15.3.19 POWER JUMPERS

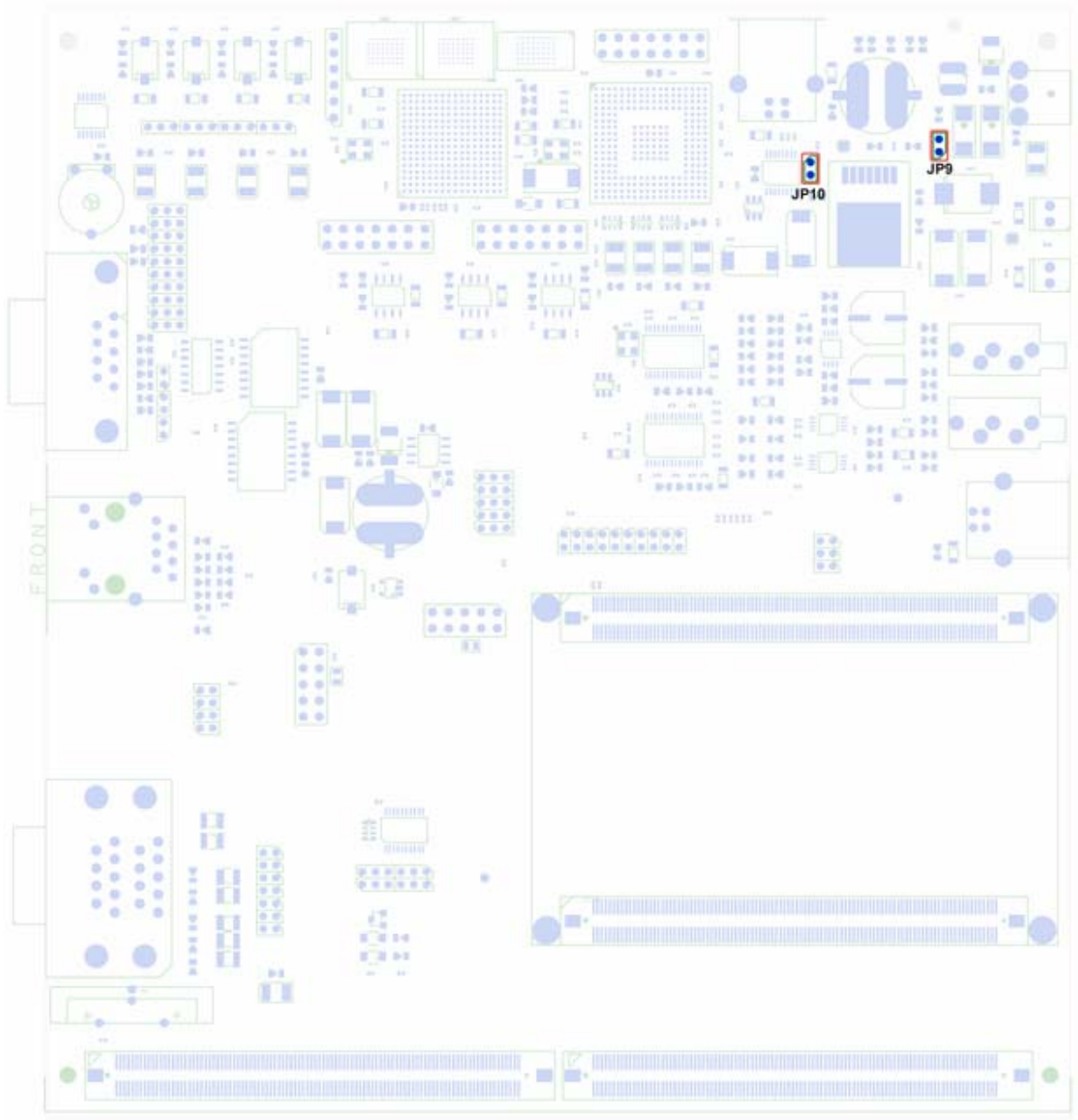

Figure 33: 5V and 3.3V current measurement jumpers

Jumpers JP9 and JP10 provide convenient access points to measure 5V and 3.3V board current. Jumper JP9 provides access to the output of the 5V power supply while JP10 provides access to the output of the 3.3V power supply. Note that JP9 and JP10 measure total board current, not current to just the phyCORE-BF537.

15.4 PIN ASSIGNMENT SUMMARY OF THE phyCORE, THE EXPANSION BUS AND THE PATCH FIELD

As described in *section 15.1* nearly all signals from the phyCORE-BF537 extend in a strict 1:1 assignment to the Expansion Bus connector X16 on the Carrier Board. These signals, in turn, are routed in a similar manner to the patch field on an optional GPIO expansion board that mounts to the Carrier Board at X16. This patch field provides easy access to all phyCORE-BF537 signals, in addition to signals generated on the Carrier Board.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X16 on the Carrier Board) as well as the patch field. However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

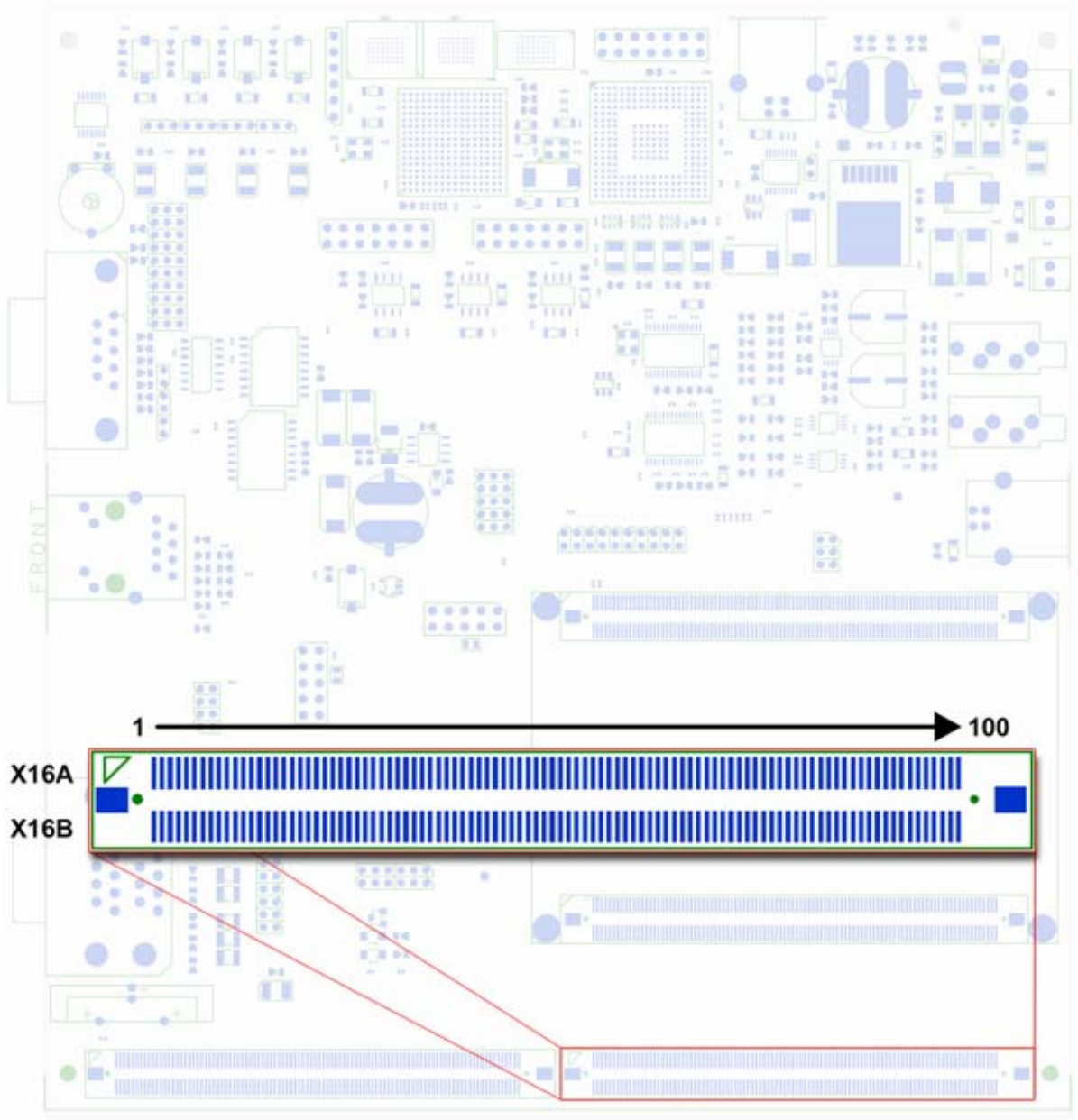

Figure 34: Pin Assignment Scheme of the Expansion Bus X16, Rows A and B

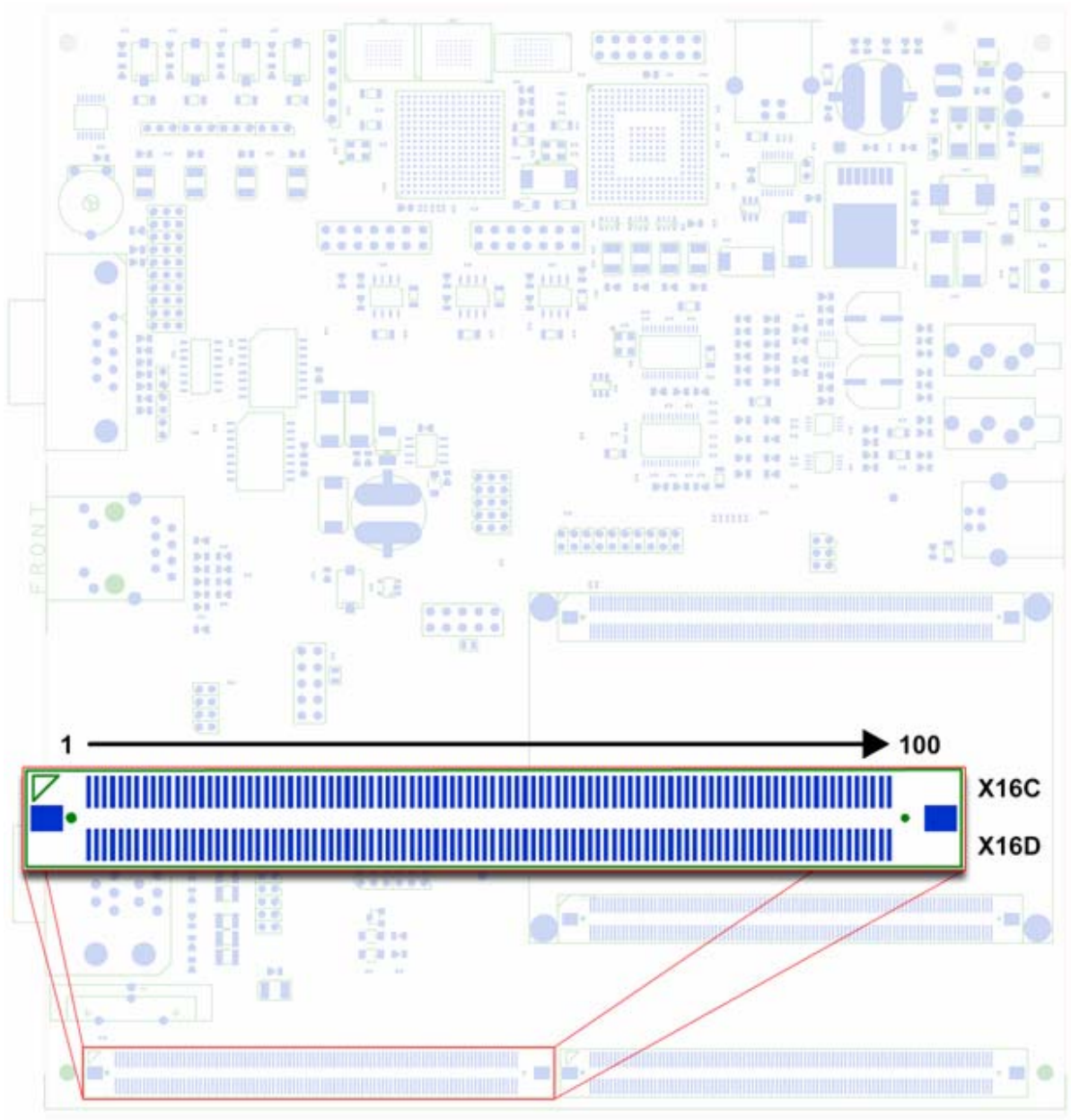

Figure 35: Pin Assignment Scheme of the Expansion Bus X16, Rows C and D

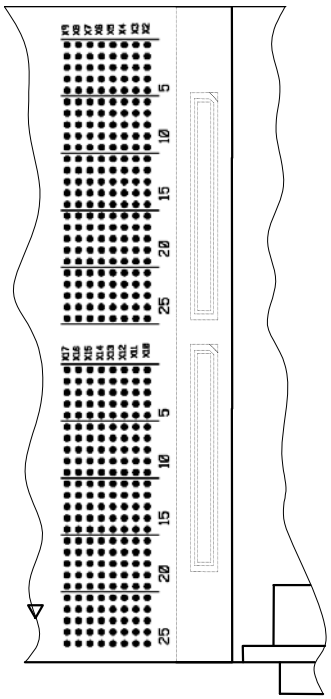

Figure 36: Pin Assignment Scheme of the Patch Field on the Optional GPIO Expansion Board

The pin assignment on the phyCORE-BF537, in conjunction with the Expansion Bus (X16) on the Carrier Board and the patch field on the optional GPIO expansion board is detailed in the following tables. Please note that the tables are arranged in functional groupings. Because there are a number of multiplex pins on the ADSP-BF537 processor, a particular pin may fall in multiple groups, and hence will be repeated in several tables.

15.4.1 System Signal Map

Table 32: System Signal Map

System			
Signal	phyCORE Module	Expansion Bus	Patch Field
/RESET	10C	10C	X9-1
/RESOUT	11C	11C	X9-2
/RESIN	10D	10D	X2-4
PWRGOOD	7D	7D	X7-1
WDI	8D	8D	X7-2
/WD_OFF	41C	41C	X2-11
CLKOUT	1B	1B	X11-1
AMS3_CTRL	25C	25C	X8-6
BMODE0	41D	41D	X3-11
BMODE1	42D	42D	X4-11
BMODE2	43D	43D	X6-11

15.4.2 Memory Bus Map

Table 33: Memory Bus Map

Memory Bus			
Signal	phyCORE Module	Expansion Bus	Patch Field
/BUF_AMS0	5A	5A	X16-1
/BUF_AMS1	5B	5B	X10-2
/BUF_AMS2	6A	6A	X17-1
/BUF_AMS3	6B	6B	X11-2
/BUF_AWE	8A	8A	X14-2
/BUF_ARE	7B	7B	X12-2
/BUF_AOE	8B	8B	X13-2
BUF_A1	9A	9A	X15-2
BUF_ARDY	34A	34A	X15-9
/BUF_ABE0	33B	33B	X13-9
/BUF_ABE1	35B	35B	X10-10
BUF_A2	10A	10A	X16-2
BUF_A3	10B	10B	X10-4
BUF_A4	11A	11A	X17-2
BUF_A5	11B	11B	X11-4

MEMORY BUS			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
BUF_A6	12B	12B	X12-4
BUF_A7	13A	13A	X14-4
BUF_A8	13B	13B	X13-4
BUF_A9	14A	14A	X15-4
BUF_A10	15A	15A	X16-4
BUF_A11	15B	15B	X10-5
BUF_A12	16A	16A	X17-4
BUF_A13	16B	16B	X11-5
BUF_A14	17B	17B	X12-5
BUF_A15	18A	18A	X14-5
BUF_A16	23B	23B	X13-6
BUF_A17	24A	24A	X15-6
BUF_A18	25A	25A	X16-6
BUF_A19	25B	25B	X10-7
BUF_D0	18B	18B	X13-5
BUF_D1	19A	19A	X15-5
BUF_D2	20A	20A	X16-5
BUF_D3	20B	20B	X10-6
BUF_D4	21A	21A	X17-5
BUF_D5	21B	21B	X11-6
BUF_D6	22B	22B	X12-6
BUF_D7	23A	23A	X14-6
BUF_D8	28B	28B	X13-7
BUF_D9	29A	29A	X15-7
BUF_D10	30A	30A	X16-7
BUF_D11	30B	30B	X10-9
BUF_D12	31A	31A	X17-7
BUF_D13	31B	31B	X11-9
BUF_D14	32B	32B	X12-9
BUF_D15	33A	33A	X14-9

15.4.3 PORT G MAP

Table 34: Port G Map

ADSP-BF537 PORT G			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
PG0	36A	36A	X17-9
PG1	37B	37B	X12-10
PG2	38A	38A	X14-10
PG3	38B	38B	X13-10
PG4	39A	39A	X15-10
PG5	40A	40A	X16-10
PG6	40B	40B	X10-11
PG7	41A	41A	X17-10
PG8	41B	41B	X11-11
PG9	42B	42B	X12-11
PG10	43A	43A	X14-11
PG11	43B	43B	X13-11
EXT_PG12	44A	44A	X15-11
EXT_PG13	45A	45A	X16-11
EXT_PG14	45B	45B	X10-12
EXT_PG15	46A	46A	X17-11

15.4.4 PORT F MAP

Table 35: Port F Map

ADSP-BF537 PORT F			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
UART0_TX (PF0)	17D	17D	X4-5
UART0_RX (PF1)	16D	16D	X3-5
UART1_TX (PF2)	20C	20C	X8-5
UART1_RX (PF3)	19C	19C	X7-5
PF4	11D	11D	X3-4
SPI_SSEL5 (PF5)	12D	12D	X4-4
/USB_RESET (PF6)	13C	13C	X5-4
/USB_IRQ (PF7)	13D	13D	X6-4
PF8	14C	14C	X7-4
PF9	15C	15C	X8-4
PF10	15D	15D	X9-4
SPI_MOSI (PF11)	16C	16C	X2-5
SPI_MISO (PF12)	18C	18C	X5-5
SPI_SCK (PF13)	18D	18D	X6-5
PF14	24C	24C	X7-6
PF15	25D	25D	X9-6

15.4.5 PORT J MAP

Table 36: Port J Map

ADSP-BF537 PORT J			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
I2C_SCL (PJ2)	31C	31C	X2-9
I2C_SDA (PJ3)	31D	31D	X3-9
CAN_RX (PJ4)	20D	20D	X9-5
CAN_TX (PJ5)	21D	21D	X3-6
PJ6	37D	37D	X4-10
PJ7	38C	38C	X5-10
PJ8	38D	38D	X6-10
PJ9	39C	39C	X7-10
PJ10	40C	40C	X8-10
PJ11	40D	40D	X9-10

15.4.6 UART Signal Map

Table 37: UART Signal Map

UART			
Signal	phyCORE Module	Expansion Bus	Patch Field
UART0_RX	16D	16D	X3-5
UART0_TX	17D	17D	X4-5
UART0_RX_RS232	22D	22D	X4-6
UART0_TX_RS232	23D	23D	X6-6
UART1_RX	19C	19C	X7-5
UART1_TX	20C	20C	X8-5
UART1_RX_RS232	21C	21C	X2-6
UART1_TX_RS232	23C	23C	X5-6

15.4.7 CAN Signal Map

Table 38: CAN Signal Map

CAN			
Signal	phyCORE Module	Expansion Bus	Patch Field
CAN_RX (PJ4)	20D	20D	X9-5
CAN_TX (PJ5)	21D	21D	X3-6

15.4.8 ADC Signal Map

Table 39: ADC Signal Map

ADC			
Signal	phyCORE Module	Expansion Bus	Patch Field
ADC_IN0	96C	96C	X2-25
ADC_IN1	96D	96D	X3-25
ADC_IN2	97D	97D	X4-25
ADC_IN3	98C	98C	X5-25
ADC_IN4	98D	98D	X6-25
ADC_IN5	99C	99C	X7-25
ADC_IN6	100C	100C	X8-25
ADC_IN7	100D	100D	X9-25
ADC_AVCC	4C, 5C	4C, 5C	X4-1, X4-2

15.4.9 CPLD Signal Map

Table 40: CPLD Signal Map

CPLD			
Signal	phyCORE Module	Expansion Bus	Patch Field
PLD_IO18	26A	26A	X17-6
PLD_IO19	26B	26B	X11-7
PLD_IO21	27B	27B	X12-7
PLD_IO22	28A	28A	X14-7
PLD_IO23	28C	28C	X5-7
PLD_IO24	29C	29C	X7-7
PLD_IO26	33D	33D	X6-9
PLD_IO27	81D	81D	X3-21
PLD_IO28	82D	82D	X4-21
PLD_IO29	83D	83D	X6-21

15.4.10 FPGA Bank 1 Signal Map

Table 41: FPGA Bank 1 Signal Map

FPGA BANK 1			
Signal	phyCORE Module	Expansion Bus	Patch Field
FPGA_B1_D5	48A	48A	X14-12
FPGA_B1_E5	49A	49A	X15-12
FPGA_B1_D4	50A	50A	X16-12
FPGA_B1_E3	51A	51A	X17-12
FPGA_B1_F3	53A	53A	X14-14
FPGA_B1_D1	54A	54A	X15-14
FPGA_B1_H6	55A	55A	X16-14
FPGA_B1_G4	56A	56A	X17-14
FPGA_B1_J2	58A	58A	X14-15
FPGA_B1_K2	59A	59A	X15-15
FPGA_B1_K4	60A	60A	X16-15
FPGA_B1_L1	61A	61A	X17-15
FPGA_B1_L2	63A	63A	X14-16
FPGA_B1_M2	64A	64A	X15-16
FPGA_B1_L3	65A	65A	X16-16
FPGA_B1_P1	66A	66A	X17-16

FPGA BANK 1			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B1_P2	68A	68A	X14-17
FPGA_B1_M4	69A	69A	X15-17
FPGA_B1_N3	70A	70A	X16-17
FPGA_B1_C1	46B	46B	X11-12
FPGA_B1_C2	47B	47B	X12-12
FPGA_B1_D3	48B	48B	X13-12
FPGA_B1_E4	50B	50B	X10-14
FPGA_B1_E2	51B	51B	X11-14
FPGA_B1_E1	52B	52B	X12-14
FPGA_B1_D2	53B	53B	X13-14
FPGA_B1_J6	55B	55B	X10-15
FPGA_B1_F5	56B	56B	X11-15
FPGA_B1_H1	57B	57B	X12-15
FPGA_B1_J1	58B	58B	X13-15
FPGA_B1_K1	60B	60B	X10-16
FPGA_B1_K5	61B	61B	X11-16
FPGA_B1_M1	62B	62B	X12-16
FPGA_B1_M3	63B	63B	X13-16
FPGA_B1_N1	65B	65B	X10-17
FPGA_B1_N2	66B	66B	X11-17
FPGA_B1_L4	67B	67B	X12-17
FPGA_B1_J4	68B	68B	X13-17
FPGA_B1_P3	70B	70B	X10-19
FPGA_B1_N4	71B	71B	X11-19

15.4.11 FPGA BANK 2 SIGNAL MAP

Table 42: FPGA Bank 2 Signal Map

FPGA BANK 2			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B2_B8	77D	77D	X4-20
FPGA_B2_D7	78D	78D	X6-20
FPGA_B2_D9	80D	80D	X9-20

15.4.12 FPGA BANK 3 SIGNAL MAP

Table 43: FPGA Bank 3 Signal Map

FPGA BANK 3			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B3_G15	43C	43C	X5-11
FPGA_B3_G16	44C	44C	X7-11
FPGA_B3_F15	45C	45C	X8-11
FPGA_B3_J11	46C	46C	X2-12
FPGA_B3_D16	48C	48C	X5-12
FPGA_B3_D15	49C	49C	X7-12
FPGA_B3_C14	50C	50C	X8-12
FPGA_B3_D14	51C	51C	X2-14
FPGA_B3_E15	53C	53C	X5-14
FPGA_B3_C15	54C	54C	X7-14
FPGA_B3_E13	55C	55C	X8-14
FPGA_B3_F14	56C	56C	X2-15
FPGA_B3_J16	58C	58C	X5-15
FPGA_B3_M12	59C	59C	X7-15
FPGA_B3_P16	60C	60C	X8-15
FPGA_B3_N16	61C	61C	X2-16
FPGA_B3_M15	63C	63C	X5-16
FPGA_B3_L16	64C	64C	X7-16
FPGA_B3_K15	65C	65C	X8-16
FPGA_B3_M14	66C	66C	X2-17
FPGA_B3_L12	68C	68C	X5-17
FPGA_B3_K13	69C	69C	X7-17
FPGA_B3_L14	70C	70C	X8-17
FPGA_B3_P14	71C	71C	X2-19
FPGA_B3_J12	52D	52D	X4-14
FPGA_B3_H12	53D	53D	X6-14
FPGA_B3_F16	55D	55D	X9-14
FPGA_B3_H11	56D	56D	X3-15
FPGA_B3_G13	57D	57D	X4-15
FPGA_B3_G12	58D	58D	X6-15
FPGA_B3_D13	60D	60D	X9-15
FPGA_B3_E14	61D	61D	X3-16
FPGA_B3_H13	62D	62D	X4-16

FPGA BANK 3			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B3_E16	63D	63D	X6-16
FPGA_B3_C16	65D	65D	X9-16
FPGA_B3_F13	66D	66D	X3-17
FPGA_B3_H15	67D	67D	X4-17
FPGA_B3_J15	68D	68D	X6-17
FPGA_B3_N12	70D	70D	X9-17
FPGA_B3_P15	71D	71D	X3-19
FPGA_B3_N15	72D	72D	X4-19
FPGA_B3_M16	73D	73D	X6-19
FPGA_B3_L15	75D	75D	X9-19
FPGA_B3_K16	76D	76D	X3-20

15.4.13 FPGA BANK 4 SIGNAL MAP

Table 44: FPGA Bank 4 Signal Map

FPGA BANK 4			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B4_N9	71A	71A	X17-17
FPGA_B4_N10	73A	73A	X14-19
FPGA_B4_R11	74A	74A	X15-19
FPGA_B4_R10	75A	75A	X16-19
FPGA_B4_K11	76A	76A	X17-19
FPGA_B4_K10	78A	78A	X14-20
FPGA_B4_P13	79A	79A	X15-20
FPGA_B4_T13	80A	80A	X16-20
FPGA_B4_T14	81A	81A	X17-20
FPGA_B4_R14	83A	83A	X14-21
FPGA_B4_L11	84A	84A	X15-21
FPGA_B4_T3	85A	85A	X16-21
FPGA_B4_P5	86A	86A	X17-21
FPGA_B4_P4	88A	88A	X14-22
FPGA_B4_R4	89A	89A	X15-22
FPGA_B4_T7	90A	90A	X16-22
FPGA_B4_L7	91A	91A	X17-22
FPGA_B4_L8	93A	93A	X14-24
FPGA_B4_R8	94A	94A	X15-24
FPGA_B4_N8	95A	95A	X16-24

FPGA BANK 4			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_B4_R6	96A	96A	X17-24
FPGA_B4_K7	98A	98A	X14-25
FPGA_B4_N6	99A	99A	X15-25
FPGA_B4_N7	100A	100A	X16-25
FPGA_B4_T11	72B	72B	X12-19
FPGA_B4_L9	73B	73B	X13-19
FPGA_B4_L10	75B	75B	X10-20
FPGA_B4_T10	76B	76B	X11-20
FPGA_B4_P12	77B	77B	X12-20
FPGA_B4_T12	78B	78B	X13-20
FPGA_B4_R12	80B	80B	X10-21
FPGA_B4_R13	81B	81B	X11-21
FPGA_B4_M11	82B	82B	X12-21
FPGA_B4_N11	83B	83B	X13-21
FPGA_B4_P11	85B	85B	X10-22
FPGA_B4_R3	86B	86B	X11-22
FPGA_B4_T4	87B	87B	X12-22
FPGA_B4_T5	88B	88B	X13-22
FPGA_B4_R5	90B	90B	X10-24
FPGA_B4_R7	91B	91B	X11-24
FPGA_B4_T8	92B	92B	X12-24
FPGA_B4_T9	93B	93B	X13-24
FPGA_B4_R9	95B	95B	X10-25
FPGA_B4_T6	96B	96B	X11-25
FPGA_B4_K6	97B	97B	X12-25
FPGA_B4_P6	98B	98B	X13-25

15.4.14 FPGA POWER AND CONTROL SIGNAL MAP

Table 45: FPGA Power and Control Signal Map

FPGA CONTROL			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
/FPGA_RST0	36B	36B	X11-10
/FPGA_RST1	35A	35A	X16-9
FPGA_PCTRL	30D	30D	X9-7
/FPGA_STATUS	30C	30C	X8-7
FPGA_VCCIO	4D, 5D	4D, 5D	X5-1, X5-2

15.4.15 FPGA JTAG SIGNAL MAP

Table 46: FPGA JTAG Signal Map

FPGA CONTROL			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
FPGA_TMS	73C		
FPGA_TDI	74C		
FPGA_TDO	75C		
FPGA_TCK	76C		

15.4.16 PPI SIGNAL MAP

Table 47: PPI Signal Map

PPI			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
PG0 (PPI Data 0)	36A	36A	X17-9
PG1 (PPI Data 1)	37B	37B	X12-10
PG2 (PPI Data 2)	38A	38A	X14-10
PG3 (PPI Data 3)	38B	38B	X13-10
PG4 (PPI Data 4)	39A	39A	X15-10
PG5 (PPI Data 5)	40A	40A	X16-10
PG6 (PPI Data 6)	40B	40B	X10-11
PG7 (PPI Data 7)	41A	41A	X17-10
PG8 (PPI Data 8)	41B	41B	X11-11
PG9 (PPI Data 9)	42B	42B	X12-11
PG10 (PPI Data 10)	43A	43A	X14-11
PG11 (PPI Data 11)	43B	43B	X13-11
EXT_PG12 (PPI Data 12)	44A	44A	X15-11
EXT_PG13 (PPI Data 13)	45A	45A	X16-11
EXT_PG14 (PPI Data 14)	45B	45B	X10-12
EXT_PG15 (PPI Data 15)	46A	46A	X17-11
PF15 (PPI Clock)	25D	25D	X9-6
/USB_IRQ (PPI Frame Sync 3)	13D	13D	X6-4
PF8 (PPI Frame Sync 2)	14C	14C	X7-4
PF9 (PPI Frame Sync 1)	15C	15C	X8-4

15.4.17 SPORT Signal Map

Table 48: SPORT0 Signal Map

SPORT0			
Signal	phyCORE Module	Expansion Bus	Patch Field
CAN_RX (SPORT0 Receive Data Secondary)	20D	20D	X9-5
CAN_TX (SPORT0 Transmit Data Secondary)	21D	21D	X3-6
PJ6 (SPORT0 Receive Serial Clock)	37D	37D	X4-10
PJ7 (SPORT0 Receive Frame Sync)	38C	38C	X5-10
PJ8 (SPORT0 Receive Data Primary)	38D	38D	X6-10
PJ9 (SPORT0 Transmit Serial Clock)	39C	39C	X7-10
PJ10 (SPORT0 Transmit Frame Sync)	40C	40C	X8-10
PJ11 (SPORT0 Transmit Data Primary)	40D	40D	X9-10

Table 49: SPORT0 Signal Map

SPORT1			
Signal	phyCORE Module	Expansion Bus	Patch Field
PG8 (SPORT1 Receive Data Secondary)	41B	41B	X11-11
PG9 (SPORT1 Transmit Data Secondary)	42B	42B	X12-11
PG10 (SPORT1 Receive Serial Clock)	43A	43A	X14-11
PG11 (SPORT1 Receive Frame Sync)	43B	43B	X13-11
EXT_PG12 (SPORT1 Receive Data Primary)	44A	44A	X15-11
EXT_PG13 (SPORT1 Transmit Serial Clock)	45A	45A	X16-11
EXT_PG14 (SPORT1 Transmit Frame Sync)	45B	45B	X10-12
EXT_PG15 (SPORT1 Transmit Data Primary)	46A	46A	X17-11

15.4.18 TWI (I²C) Signal Map

Table 50: TWI (I²C) Signal Map

TWI (I²C)			
Signal	phyCORE Module	Expansion Bus	Patch Field
I2C_SCL	31C	31C	X2-9
I2C_SDA	32D	32D	X4-9
I2C_WP	31D	31D	X3-9

15.4.19 Power Signal Map

Table 51: Power Signal Map

POWER			
Signal	phyCORE Module	Expansion Bus	Patch Field
VCC	1C, 2C, 1D, 2D	1C, 2C, 1D, 2D	X2-1, X2-2, X3-1, X3-2
ADC_AVCC	4C, 5C	4C, 5C	X4-1, X4-2
FPGA_VCCIO	4D, 5D	4D, 5D	X5-1, X5-2
VBAT	6C	6C	X6-1
VPD	6D	6D	X6-2
AGND	82C, 87C, 92C, 97C, 84D, 89D, 94D, 99D	Connected to GND	Connected to GND
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	X2 through X17 – 3 X2 through X17 – 8 X2 through X17 – 13 X2 through X17 – 18 X2 through X17 - 23

Table 52 below lists additional signals that are generated on the Carrier Board. Since these signals originate on the Carrier Board, they have no applicable connection to the phyCORE-module.

Table 52: Carrier Board Generated Signal Pin Assignment for the phyCORE-BF537 / Carrier Board / Expansion Board

CARRIER BOARD GENERATED SIGNALS			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
LED1	N/A	88C	X5-22
LED2	N/A	89C	X7-22
LED3	N/A	90C	X8-22
LED4	N/A	91C	X2-24
BTN1	N/A	87D	X4-22
BTN2	N/A	88D	X6-22
BTN3	N/A	90D	X9-22
BTN4	N/A	91D	X3-24
ADC_INx	N/A	95D	X9-24
ADC_AVCC2	N/A	95C	X8-24

Table 53: Unused Pins on the phyCORE-BF537 / Carrier Board / Expansion Board

UNUSED PINS			
SIGNAL	phyCORE MODULE	EXPANSION BUS	PATCH FIELD
NC	1A, 3A 2B, 3B, 100B 8C, 9C, 83C, 84C, 85C, 86C, 88C, 89C, 90C, 91C, 93C, 94C, 95C 85D, 86D, 87D, 88D, 90D, 91D, 92D, 93D, 95D	1A, 3A 2B, 3B, 100B 8C, 9C, 26C, 33C, 34C, 35C, 36C, 73C, 74C, 75C, 76C, 78C, 79C, 80C, 81C, 83C, 84C, 85C, 86C, 93C, 94C 27D, 28D, 35D, 36D, 45D, 46D, 47D, 48D, 50D, 51D, 85D, 86D, 92D, 93D	X10-1, X14-1 X12-1, X13-1, X17-25 X8-1, X8-2, X2-7, X5-9, X7-9, X8-9, X2-10, X5-19, X7-19, X8-19, X2-20, X5-20, X7-20, X8-20, X2-21, X5-21, X7-21, X8-21, X2-22, X5-24, X7-24 X4-7, X6-7, X9-9, X3-10, X9-11, X3-12, X4-12, X6-12, X9-12, X3-14, X9-21, X3-22, X4-24, X6-24

16 REVISION HISTORY

Date	Version numbers	Changes in this manual
01-Mar-2007	Manual L-696e_0 PCM-033 PCB# 1256.1 PCM-975 PCB# 1257.1	First draft, Preliminary documentation. Describes the phyCORE-Blackfin/BF537 and Carrier Board
22-May-2007	Manual L-696e_1 PCM-033 PCB# 1256.1 PCM-975 PCB# 1257.2	First release version. Description added in Passive FPGA Configuration section.

17 COMPONENT PLACEMENT DIAGRAM

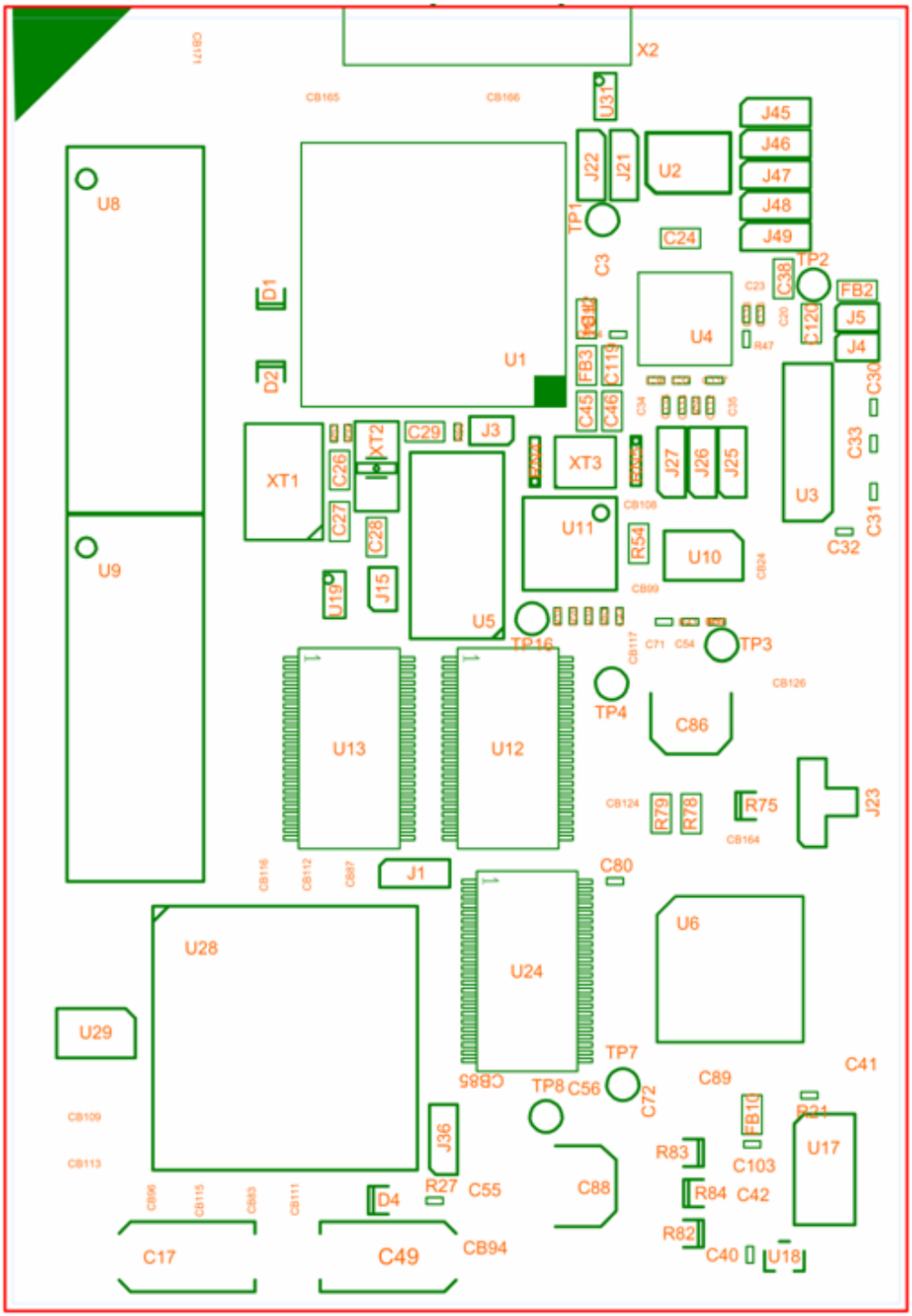

Figure 37: phyCORE-BF537 Component Placement, Top View

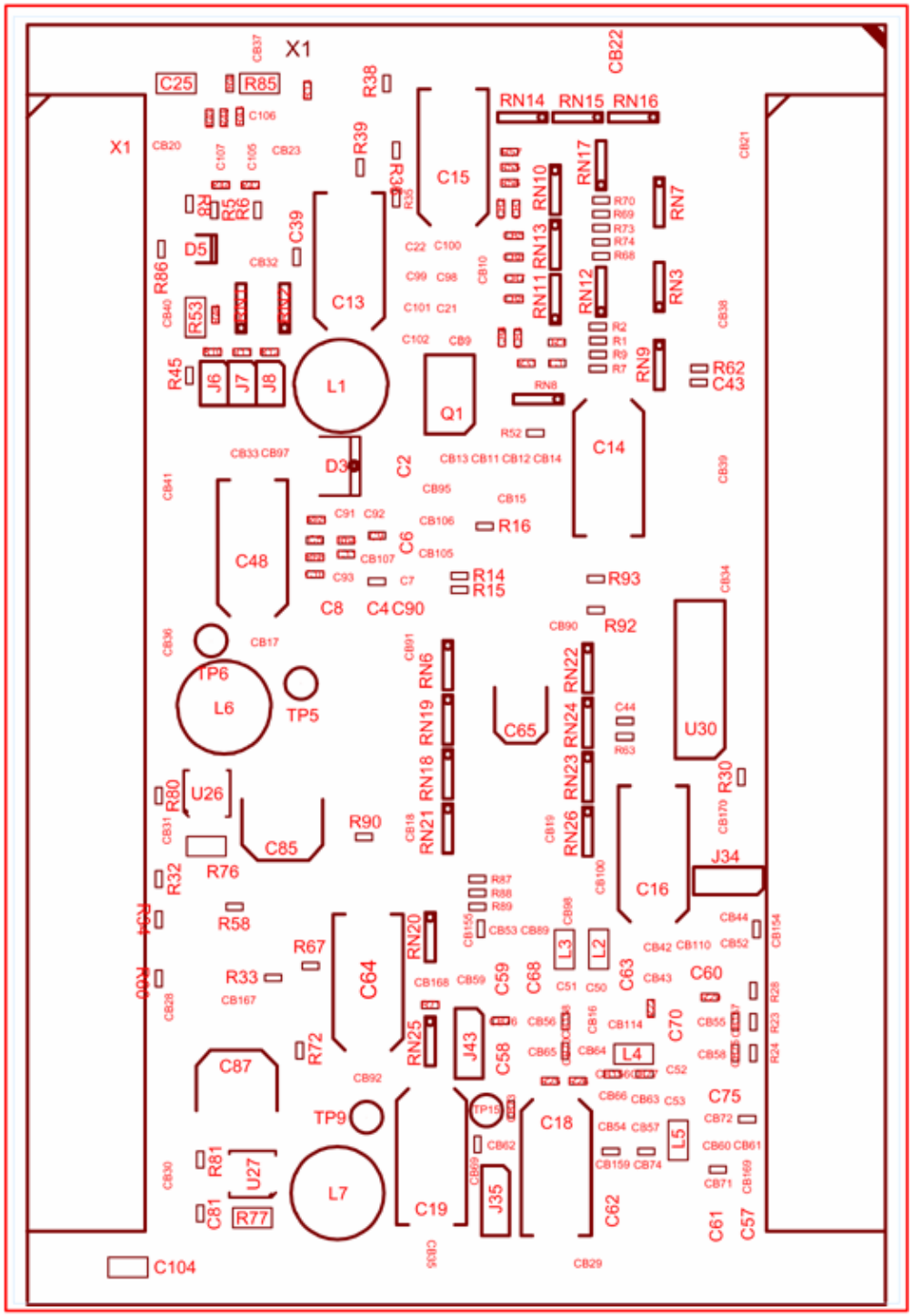

Figure 38: phyCORE-BF537 Component Placement, Bottom View

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Document:	**phyCORE-BF537 Hardware Manual**
Document number:	**L-696e_1, May 2007**

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Did you find any mistakes in this manual? page

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